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Final Report
to
Office of Naval Research
of
A Program of Research
on

Physical Concepts and Modeling Procedures for Picosecond and Subpicosecond Distributed Circuits

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Principal Investigators

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I. Introduction

The development of advanced high-speed digital devices and integrated circuits has been spurred by a number of applications, including fiber-optic digital data transmission at gigahertz rates, high-throughput computing, and wideband signal processing. Military interest in high-speed digital electronics stems from the need to rapidly acquire, digitize, and process very large amounts of data in EW systems. Associated with the needs for high-speed logic are commensurate demands for broadband analog signal processing, interface, and I/O electronics. Such circuits include correlators, broadband adaptive filters, picosecond-resolution sample-and-hold gates, and multigigahertz-rate D/A and A/D converters. For the digital and analog circuits mentioned, ultra-wide bandwidth instrumentation of superior speed is required for measuring the devices to be employed.

It is primarily this critical need for ultra-wide bandwidth instrumentation that has been addressed through the work done under this contract. Without such a capability for performing picosecond and subpicosecond measurements of electrical phenomena, it will be impossible to correctly engineer and characterize devices and circuits required for the applications listed above.

While we give only the highlights of the results achieved during work on this contract, details of the theory and design used in constructing the instrumentation, as well as the fabrication techniques employed, are fully discussed in an Appendix, consisting of the entire dissertation of R. A. Marsland on the integrated circuit sampler technology developed under this contract.

II. Progress Under Contract

Picosecond Pulse Generators and Sampling Circuits

We have developed monolithic circuits for both picosecond pulse generation and sampling of repetitive waveforms, with bandwidths extending to 290 GHz. The circuits used to strobe these samplers are nonlinear transmission lines (NLTLs),[1] high-impedance coplanar waveguide transmission lines periodically loaded with reverse-biased Schottky diodes, which steepen the falling portion of a sinusoidal excitation on the line to a brief (1.6 ps) 10%-90% falling edge. The samplers developed under this contract[2] are two-diode sampling bridges which are strobed by the derivative of the NLTL's falling edge, which is approximately an impulse function. We have also used these samplers in a monolithic Wheatstone bridge[3] for measuring vector parameters of waves (e.g. S-parameters) in high-speed devices. Incorporating this bridge into a coplanar waveguide probe, we were able to calibrate and make measurements to 78 GHz, limited only by availability of frequency extenders for the network analyzer we were using.

Previously, we had reported a diode sampling bridge monolithically integrated with a NLTL strobe-pulse and test-signal generators which had a sampling bandwidth of over 130 GHz. This sampler measured a 4 ps fall time from the attenuated output of the on-chip NLTL test-signal generator. The speed-limiting factors in this circuit were sampling diode series resistance and NLTL transition times themselves. The series resistance was high due to the relatively thick N^- layer used for the varactor diodes of the on-chip NLTL. This problem was remedied in later generations by going to a two-chip solution in which the first part of the edge-sharpening from a microwave sinusoid to a sawtooth wave was accomplished one one chip with a hyperabrupt-doped NLTL, giving a 5 ps falling edge. The final edge steepening was performed on the second chip with an abrupt-doped sampling IC, where varactor breakdown was not as critical because of lower signal amplitudes. This allowed a thinner N^- layer to be employed in the sampler, reducing the series resistance of the sampling diodes.

To increase the speed of the sampler, improvements were made to the NLTL, the sampling diode epitaxial structure, and overall IC layout. The portion of the NLTL which was integrated on the sampling chip was designed to have a periodic cutoff frequency of

500 GHz, as discussed in the Appendix, Ch. 3. With the other improvements, the completed sampler exhibited better than twice the first-generation sampler's bandwidth.

Modeling

Our ability to model complex, high-frequency structures, such as those designed and built under this contract, has been enhanced by the acquisition of important CAD tools, running on a RISC-based UNIX workstation. We have entered into agreements with Meta-Software (makers of HSPICE, a sophisticated and powerful version of SPICE), with CONTEC Microelectronics (also makers of a version of SPICE with good transmission-line models), and with Sonnet Software (makers of em, an electromagnetic structure simulator for arbitrary geometries.)

Both versions of SPICE we have currently offer significantly improved transmission-line models over the standard delay-based model used in Microwave SPICE from eesof. These models incorporate both loss and dispersion, as well as arbitrary coupling between lines. Hence, they allow us to more accurately model NLTLs and samplers, a necessity for second- and third-order improvements in performance. In addition, HSPICE offers numerical optimization of parameters.

Em calculates the S-parameters for arbitrary microstrip or coplanar waveguide geometry with high accuracy for all microwave frequencies. It solves for the current distribution in the metallization, including all dispersion, stray coupling, discontinuities, surface waves, moding, metalliztion loss, dielectric loss, and radiation loss. It, too, will enable us to further improve our designs.

III. Conclusion

We have demonstrated ultra-wide bandwidth time- and frequency-domain instrumentation which can be monolithically integrated and used to 300 GHz for measuring ultrafast electrical phenomena. Work will continue along the directions we have mapped out in order to bring increased bandwidth and accuracy to the instruments we have developed and disclosed.

IV. Technology Transfer

The NLTL and sampler technologies are already finding applications in industry and exist in 4-6 products: Licensing agreements have been signed with Tektronix and Yokogawa Electric Corp. concerning both technologies. Although negotiations are only beginning with Hewlett-Packard, they have already put the NLTL to use as a strobe generator in their HP-54124T 50 GHz sampling oscilloscope.[4]

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GALLIUM ARSENIDE INTEGRATED CIRCUITS FOR MEASUREMENT AND GENERATION OF ELECTRICAL WAVEFORMS TO 300 GHZ

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
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FOR THE DEGREE OF
DOCTOR OF PHILPSOPHY

By
Robert A. Marsland, Jr.
June 1990

Abstract

Until the advent of the monolithic nonlinear transmission line (NLTL), high-speed samplers found in oscilloscopes, network analyzers, frequency counters, frequency synthesizers, and spectrum analyzers were based on the step recovery diode (SRD) and a sampling bridge requiring hybrid assembly. SRD technology is quite mature and switching speeds much faster than $\sim$ 20ps cannot be expected. Because sensitivity can be traded for speed to some degree, instruments based on this technology have reached 60 GHz. The NLTL and monolithic sampling bridge exploiting $> 1THz$ cutoff frequency diodes with no package or interconnect parasitics offer a dramatic improvement in bandwidth over the SRD hybrid technology, or similarly, increased sensitivity with similar bandwidth.

As has been shown previously, the shock wave output of a NLTL can have a fall-time of less than 1.6 ps. This thesis presents the first applications of this technology in conjunction with monolithic diode sampling bridges for mm-wave instrumentation to 300 GHz. A two-diode sampling bridge has been monolithically integrated with a NLTL as the strobe pulse generator to achieve a sampling bandwidth of over 290 GHz. In addition, two sampling bridges have been integrated with a resistive directional bridge to form a 60 GHz S-parameter test-set on a chip. The use of a NLTL for phase-matched frequency doubling is also discussed.

These integrated circuits not only provide a dramatic improvement in performance, but also the possibility of mass-production and lower cost of assembly due to reduced part count. In addition, because of their small size, it is possible to mount the integrated circuits on probe tips to provide on-wafer measurement capability to 300 GHz without the reduced sensitivity and directivity caused by coaxial cables.

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I dedicate this dissertation to my wife Diane, whose patience and encouragement allowed me to complete it in a timely fashion.

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Chapter 1

Introduction

1.1 Broad-band instrumentation

This thesis focuses on the application of GaAs integrated circuits to test instrumentation. This is appropriate since test instruments in general must be superior in performance to the systems or devices that are being tested; therefore, it is here that most high-performance circuits find their first, and sometimes only, application. Here *high-performance* can mean either high-speed or high-frequency. Such nomenclature can be confusing, as researchers working on the next generation of computers want an instrument that can measure fast transients (high-speed) while microwave and mm-wave engineers want broad-bandwidth (high-frequency) instrumentation. The primary distinction is that a large *instantaneous* bandwidth is necessary for time-domain applications while those thinking and working in the frequency domain typically only require operation at a single frequency, provided the instrument can be rapidly adjusted to operate at a new frequency or set of frequencies. Optical communication systems defy even this loose definition since the fractional optical bandwidth is extremely small, yet very high-speed signals are transmitted. In this thesis, *broad-band* will describe a circuit, device, or instrument that provides either an instantaneous or adjustable bandwidth that is exceptionally large.

Most broad-band instruments first convert the waveform to be analyzed to a lower frequency before performing analysis. Sampling is preferred for this purpose

since conversion loss is independent of the local oscillator (LO) harmonic number, allowing a single low frequency low cost LO to be used for rf frequencies ranging from 1 to over 100 times the LO frequency. Another advantage of the 'flat' conversion loss is that periodic, non-sinusoidal waveforms may also be down-converted with low distortion. A general sampling system block diagram is shown in Fig. 1.1. The

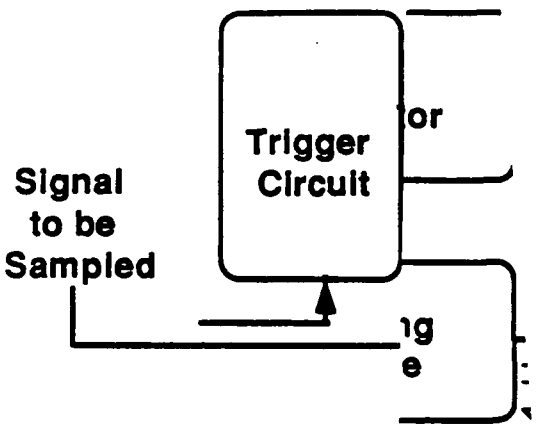

Figure 1.1: General sampling system block diagram. When the sampling device receives a pulse, a short sample is taken of the input signal. The phase relationship between the signal and the pulse generator is controlled by the trigger circuit.

trigger circuit detects a threshold crossing and, after a subsequent delay, sends a trigger pulse to the pulse generator, which turns on the sampling gate to take a short sample of the signal. If the trigger circuit generates the same delay after every threshold crossing, the same point in the rf signal will always be sampled and the hold capacitor will eventually charge up to the full rf voltage at this point in the waveform. If the trigger delay increases by a fixed amount between samples, the voltage on the hold capacitor will trace out the rf waveform at a lower frequency. The most obvious application of the sampling system is for the viewing of repetitive, high-speed waveforms. However, samplers find their way into many instruments.

Samplers can be found in sampling oscilloscopes, vector network analyzers, frequency synthesizers, spectrum analyzers, and frequency counters. Currently, the oscilloscope with the greatest bandwidth is the Hewlett-Packard (HP) 54124T which has a 3-dB bandwidth of 50 GHz [1.1]. This oscilloscope and its 34 GHz predecessor represent the first industrial application of the monolithic nonlinear transmission line (NLTL) technology developed by Rodwell and Madden [1.2,3] and discussed in §1.2.2. Wiltron, on the other hand, boasts the vector network analyzer with greatest bandwidth (60 GHz) using a conventional step-recovery-diode (SRD). Since the network analyzer measures normalized parameters, the samplers can be used well above their 3-dB bandwidth. The upper frequency limit is reached only when the signal-to-noise ratio at the receiver becomes unacceptable.

A simplified network analyzer block diagram is shown in Fig. 1.2. The automatic network analyzer (ANA) block diagram is very similar to that of the sampling oscilloscope. In fact, the same sampler design can be used for both applications. The major difference, besides the additional rf components of the ANA, is that the oscilloscope is a very general instrument and so few assumptions may be made about the input signal. So, typically, every sample must be individually processed. The ANA has a very specific task, which it is optimized to perform: the measurement of S (scattering)-parameters. In this case, the samples are not individually processed but rather integrated on a hold capacitor as in Fig. 1.1. The samplers used in frequency synthesizers, frequency counters, and spectrum analyzers are used as frequency converters, as in the ANA. The samplers studied in this thesis work were evaluated in terms of both ANA and oscilloscope applications.

1.2 Recent advances in broad-band measurement

This section briefly describes two new technologies which provided the motivation for this thesis work: electrooptic sampling and the nonlinear transmission line. Electrooptic sampling with its tremendous bandwidth issued a challenge: what electronic device can be fast enough to require such bandwidth? The nonlinear transmission line responded and in doing so made possible an all-electronic sampler with

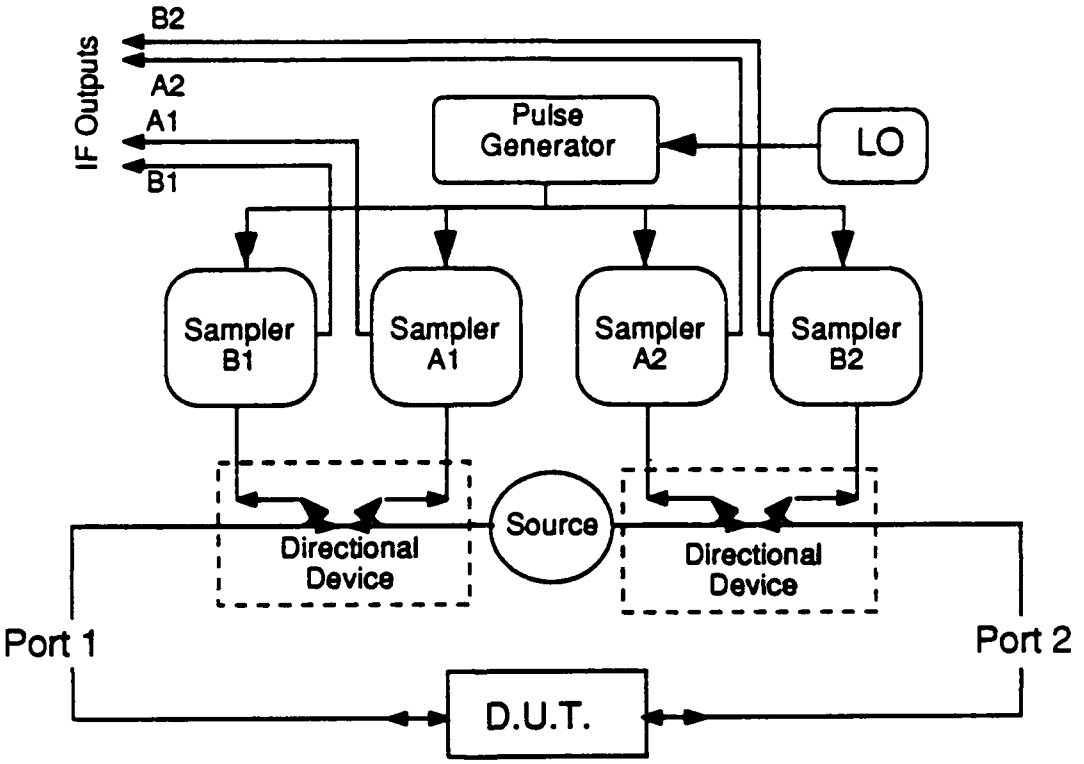

Figure 1.2: Simplified automatic network analyzer block diagram. Directional couplers send portions of the incident and reflected signals to the four samplers where they are down-converted to an intermediate frequency (IF) for further processing.

even greater bandwidth. The all-electronic sampler, its applications, and variations on the nonlinear transmission line are the subjects of this thesis. A description of electrooptic sampling and the nonlinear transmission line is included here for completeness.

1.2.1 Electrooptic sampling

Electrooptic (EO) sampling is an optical probing technique that takes advantage of the short pulse width available from an ultra-fast pulsed laser to provide temporal

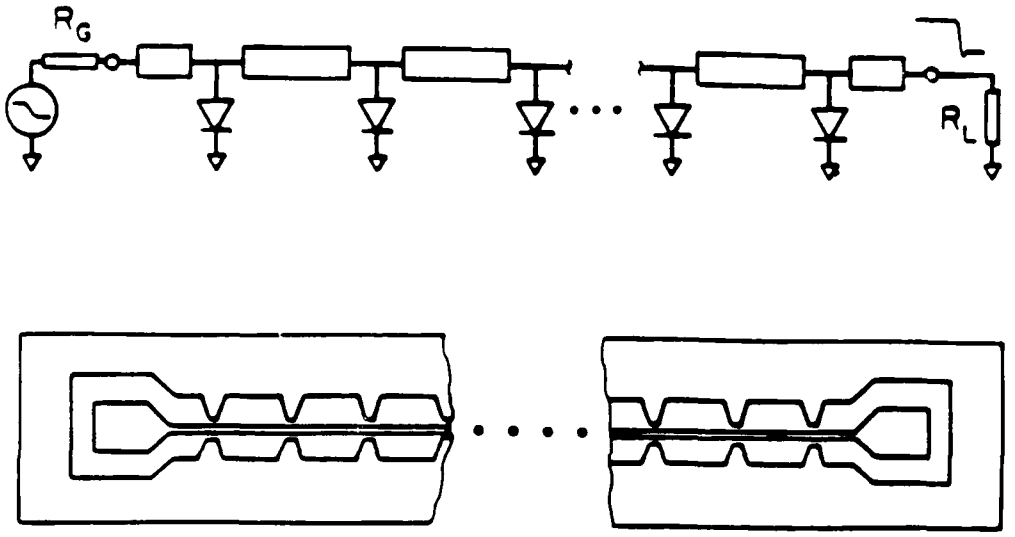

Figure 1.3: Nonlinear transmission line schematic diagram. The inductance of the series high impedance transmission lines and the capacitance of the reverse biased diodes forms a synthetic transmission line with a propagation velocity that is a function of voltage. After Rodwell et al.

resolution on the order of 1 ps or less. The optical beam can interact with an electrical signal by passing through an EO crystal brought sufficiently close to the signal conductor to sense its electric field [1.4,5,6]. Alternatively, when the conductor to be probed is patterned on an electrooptic substrate such as GaAs, the substrate itself can provide the EO interaction [1.7]. The latter technique was developed by Weingarten and Rodwell [1.8,9,10] into a system which can provide internal node probing of GaAs integrated circuits under realistic excitation and loading conditions with a bandwidth of approximately 200 GHz. This system was used extensively for evaluating the circuits described in this thesis.

1.2.2 The nonlinear transmission line

The nonlinear transmission line (NLTL), shown schematically in Fig. 1.3, is a relatively high impedance transmission line periodically loaded with reverse biased

Schottky diodes serving as voltage-dependent shunt capacitances [1.11,12,13]. Because the capacitance decreases with increasing reverse bias, the phase velocity of a small signal will be slower when the line is biased near zero volts than when it is strongly reverse biased. If a large gradual-step signal is applied to the line, points on the waveform with amplitude near zero will experience a greater delay than the more negative portion. Therefore, the step will tend to steepen as it propagates. The simulated NLTL waveforms in Fig. 1.4 illustrate this process, known as shock-

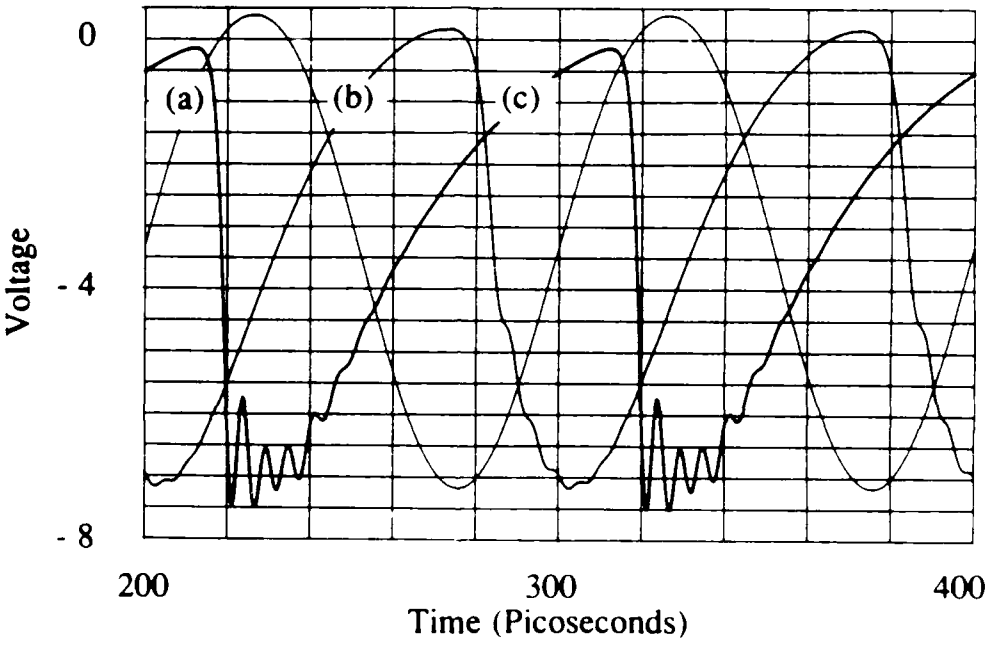

Figure 1.4: Simulation of voltage waveforms at various positions on a NLTL. The input is a 10 GHz $8V_{pp}$ sinusoid (a). After 15 diode sections, a shock-wave begins to form near zero volts (b). After 30 diodes, shock wave formation is nearly complete (c). Figure courtesy of C.J. Madden.

wave formation. A comparison of waveforms (a) and (b) shows that the portion of the waveform near zero volts, where the change in delay is greatest, steepens first. At point (c) the entire falling edge has been sharpened. The steepening process continues until spreading due to dispersion just balances the compression arising from the nonlinear capacitance.

The two dominant sources of dispersion are line periodicity and device parasitics.

If the diodes are close enough together, so that the filter cutoff is high, the bandwidth of the line will be limited by the RC time constant of the diodes rather than the filter cutoff. Since Schottky diodes have been fabricated with RC time constants as low as 18 fs [1.14], there is the potential for subpicosecond falltimes. The *monolithic* NLTL circuit [1.2,3] is implemented in coplanar waveguide to reduce the parasitic inductance of the shunt diode connection. Processing is also simplified since vias and back-side metalization are not required.

The monolithic NLTL is fabricated on semi-insulating GaAs with the active layers grown by molecular-beam epitaxy. A heavily doped N^+ buried layer provides the diode cathode connection and shorts the two ground planes of the CPW together to suppress the unwanted even CPW mode. The doping profile of the top N^- layer determines the capacitance and resistance per unit area of the diode. This profile is tailored to provide the lowest RC time constant possible, while achieving the desired change in capacitance with voltage.

1.3 Overview of this thesis

The major contributions of this thesis include:

- First application of the monolithic nonlinear transmission line technology to high-speed sampling.
- Fastest all-electronic sampler (< 1.6 ps risetime).
- First monolithically integrated directional bridge with samplers.
- Generation of 100-110 GHz radiation by phase-matched frequency multiplication on a NLTL.

The process technology which is common to all ot the ICs of this thesis is described in Chapter 2. Sampling theory and the three design iterations on monolithic sampling bridges are discussed in Chapter 3. The monolithic integration of two samplers with a directional bridge is presented in Chapter 4. Phase matched second harmonic generation of a nonlinear transmission line is studied theoretically

with coupled-mode theory and experimentally by electrooptic sampling in Chapter 5. The conclusion and some possible future work are contained in Chapter 6.

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Chapter 2

GaAs processing

2.1 Introduction

The bandwidth of the circuits discussed in this thesis relies, at least in part, on the RC cut-off frequency of the Schottky diodes. Low-loss transmission lines, airbridge interconnects, and N^+ resistors are also required. In addition, it is important to understand the constraints imposed by the process technology before a circuit design is finalized. Very often a small change in the circuit design which has a minimal impact on the circuit function but will greatly increase the yield of the completed circuits. Similarly, there may be a small adjustment in the physical layout which significantly improves the high-frequency circuit performance. An understanding of the process constraints and their origins allows the proper balance to be struck between circuit performance, yield, and processing difficulty. This chapter contains a description of the process developed to satisfy these demands. Monolithic diode fabrication steps developed by Rodwell and Madden [2.1,2] are discussed first. Airbridges and metal-insulator-metal capacitors added for the purposes of this thesis are described next. Design rules are described in the last section. The entire process was developed in accordance with standard industry practices to keep things simple and facilitate technology transfer.

2.2 Diode fabrication

The starting material for this process is semi-insulating [100] GaAs polished on both sides to allow EO sampling by backside probing (see §1.2.1). The active layers consist of a heavily doped N^+ layer and a more moderately doped N^- layer grown by molecular-beam-epitaxy (MBE). The underlying N^+ layer, typically 0.8 μm thick, provides the diode cathode connection, while the N^- layer determines the capacitance and resistance per unit area of the diode. This profile is tailored to provide the lowest RC time constant possible, while achieving the desired change in capacitance with voltage. With the thick layers required for Schottky diodes, other epitaxial techniques may be used, but MBE material is readily available because of our collaboration with Yi-Ching Pao of Varian III-V Device Center. Specific diode designs are discussed in later chapters.

A typical Schottky plan-view and cross-section are shown in Fig. 2.1. The layer structure shown in this figure was used for sampler Generations I and II but was modified for Generation III. Ohmic contacts are formed by etching down to the N^+ layer and performing a self-aligned liftoff of 108Å Ge/102Å Au/63Å Ge 236Å Au/100Å Ni/xÅ Au, where x is the thickness required to fill the etch-well. After liftoff, the contacts are annealed for 25 seconds at 450°C. Isolation between diodes is achieved with a multienergy proton implant. During implantation, the active areas are protected by 1.8 μm of Au on 1.4 μm of polyimide. Isolation provided by the proton damage is > 40M $\Omega/\square$. After implant, the Au mask is stripped by dissolving the polyimide in its solvent.

Schottky contacts and interconnects are simultaneously patterned with a liftoff of 1000Å Ti/750Å Pt/1.4 μm Au. Schottky diodes are formed where the center conductor crosses over an undamaged active region. Using the same metalization for Schottky contacts as interconnect metal saves one mask step and the need for alignment. Unfortunately, it is difficult to make small (< 2 μm) diodes, since the interconnect metal must be thick for low microwave loss. For the very highest performance sampler described in §3.3.3, the patterning was separated into two mask steps. A thin metal was used for the small geometry diodes while a thick metal with

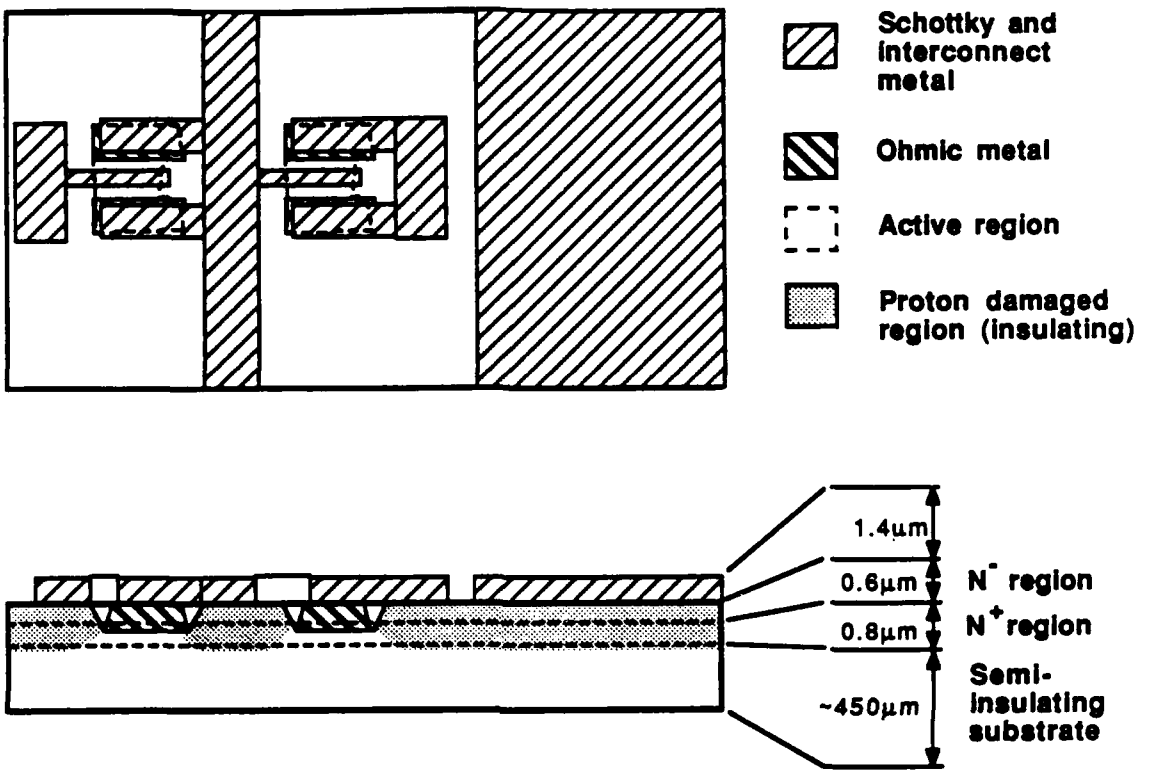


Figure 2.1: Two Schottky diodes are shown in plan-view (top) and cross-section (bottom). The layout shown here is typical for switching diodes.

lower titanium content was used for interconnect metal.

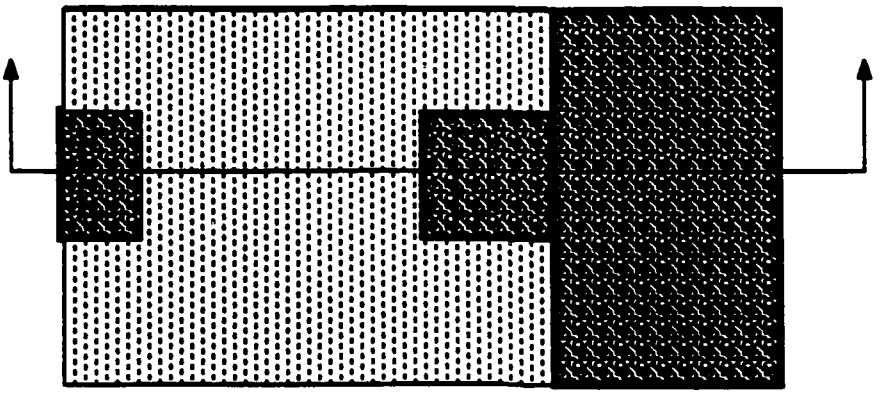
2.3 Capacitors and airbridges

The three masks steps of the diode fabrication process of §2.2 are sufficient for nonlinear transmission line fabrication, but metal-insulator-metal (MIM) capacitors and airbridges are needed to add a sampling bridge. Silicon nitride (also called just *nitride* or Si_3N_4), deposited by plasma-enhanced chemical vapor deposition (PECVD) was chosen as the capacitor dielectric because it has a high dielectric constant ~ 7.3, provides some scratch protection, and is used extensively in industry.

The nitride must be deposited at relatively low temperature to avoid degradation of the Schottky junction [2.3]. At a deposition temperature of 290°C the Schottky diode breakdown voltage was reduced from 18 V to 10 V. At 350°C, the breakdown voltage was reduced to 4 V. Deposition temperatures below 275°C caused only small ($\sim 1V$) degradation. Producing high quality nitride at such a low temperature is difficult. However, Gerald Li, then at Varian III-V Device Center, had already developed a low-temperature nitride process and was willing to perform the deposition himself. Nitride can be etched with hydrofluoric or phosphoric acid solutions [2.4]. Unfortunately, the etch rate is low ($\sim$ 10Å/min) and the titanium sticking layer used for the Schottky contacts is attacked. Dry-etching in a C_2F_6 plasma, on the other hand, provides very reasonable etch rates ($\sim$ 300Å/min) without significant damage to other films on the substrate. Surface damage due to physical sputtering is not a problem since the active regions are protected by metal or photoresist or both.

Once contact holes have been opened through the nitride, a 1.6 μm layer of photoresist is patterned to define where airbridges will contact the underlying metal (Fig. 2.2). This resist is hard-baked for 20 minutes at 120°C to cause the resist to flow slightly and provide sloping resist sidewalls. A 100ÅTi / 2000ÅAu / 300ÅTi film is then evaporated. This metal will be the current carrying layer for later electroplating. The titanium layers improve adhesion to the photoresist above and below. The thick gold layer is necessary to avoid breaks at resist edges. A thinner layer could be used if it was sputtered rather than evaporated. Finally, a 4 μm layer of resist defines where the thin gold layer is to be plated.

The 300Å layer of Ti is etched in a weak (10:1) $H_2O : HF$ solution immediately prior to plating. This keeps the gold vacuum clean until it is ready to be plated. Once the gold is exposed, it is plated to a thickness of 2.3 to 3.0 μm . After plating, the upper level resist is removed by spraying the surface with acetone. The Ti/Au/Ti film is then removed with weak HF and gold etchants. Finally, the underlying resist is removed with an overnight soak in acetone. The completed structure is shown in Fig. 2.3.



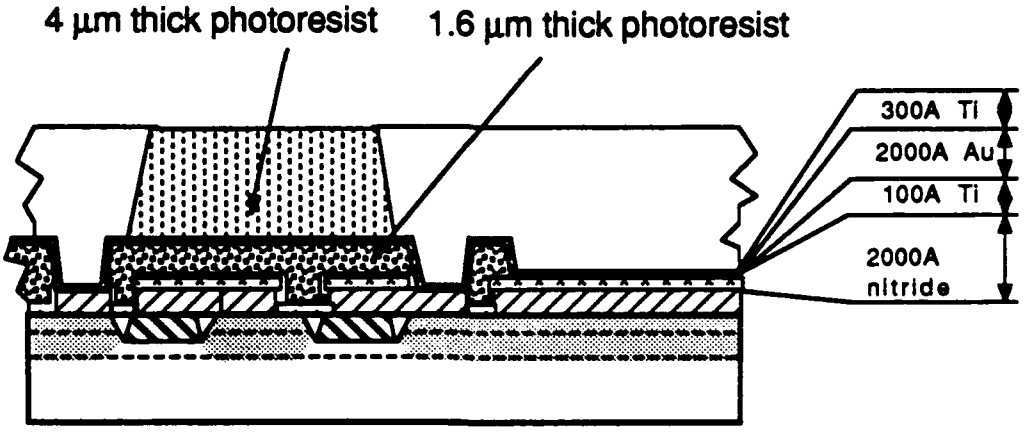


Figure 2.2: Airbridge and MIM capacitor process. The lower layer of resist defines where the airbridges will contact the underlying metal or nitride and acts as a temporary support for the metal which is evaporated next. The final layer of photoresist defines the regions to be plated.

2.4 Design rules

Designing an integrated circuit to minimize the effects of parasitics often results in layout geometries which are difficult to fabricate. Therefore, it is important to understand the constraints imposed by the fabrication process before committing to a particular design. It is usually better to design around a process problem than to process around a design problem.

Ohmic contacts to the 0.8 μm N^+ layer doped $3\times10^{18}cm^{-3}$ prepared by alloying a Au/Ge/Ni/Au film, as described in §2.2, routinely achieve 0.035 Ωmm contact resistance with a standard deviation of 0.015 Ωmm over the wafer. The sheet resistance of the N^+ layer is typically 9.6 $\Omega/\square$ with a standard deviation of 0.4 $\Omega/\square$ across the wafer although actual resistance can vary with the width of the active region. In three wafer runs, the average sheet resistance of the N^+ layer was 8.6, 11.7, and 9.6 $\Omega/\square$ for an overall average of 10 $\Omega/\square$ and a deviation of 1.6 $\Omega/\square$. The active region width dependance is most likely because the protons can "straggle" underneath the implant mask, reducing the width of the undamaged region (Fig. 2.4). In practice, a 5 μm wide resistor has a resistance per square of N^+ material that is approximately 20% higher than a 100 μm wide resistor. This indicates a proton straggle of approximately 0.5 μm on each side, which is approximately 50% of the vertical proton projected range.

If allowance is made for straggle, the major source of error in resistance values will be due to variation in contact resistance. To minimize this effect, the contacts should be made as large as possible. For example, a 50 Ω resistor designed to have 5 μm wide ohmic contacts and use 3 squares of material would have a tolerance of

$$2\frac{0.035\ \Omega mm}{0.005mm} \times 43\% + 3\square \times 12\ \Omega/\square \times 16\% = 24\%$$

whereas a resistor with 20 μm wide ohmic contacts and 4.6 squares of material would have a 18% tolerance.

Another problem with small ohmic contacts is that they tend to fail at approximately 17 mA/ μm of design width. This failure is probably due to electron velocity saturation at some point in the resistor. Any additional voltage beyond the onset of saturation will drop across the region of saturated velocity. Power dissipation

will therefore increase in this small region until the power density exceeds what the material can bear. Assuming an elevated temperature saturation velocity of $0.5 \times 10^7 cm/s$ [2.5] and a cross-sectional area of

0.65 μm (N^+thickness – ohmic recess over-etch) $\times$ 3 μm (ohmic contact width)

gives a saturation current of 47 mA. This agrees well with the observed failure of a 3 μm ohmic at 55 mA after saturating at 50 mA.

The small capacitors required in high-frequency circuits do not present nearly the design problem as resistors. When the nitride thickness is greater that 1000Å, shorts through pin-holes in the nitride are not a problem for capacitors smaller than 2 pF. It is important, however, to keep the top plate of the capacitor away from the edge of the bottom plate to avoid possible voids in the nitride on the metal edge.

The remaining design rules are related to lithography. For thick metal lift-off [2.1] used for interconnect metal, the minimum line width and space are 2 and 3 μm , respectively. Thin metal, which was added for the Generation III sampler, can achieve 1 μm lines and 2 μm spaces. Airbridge metal can only attain 5 μm lines and spaces because of the very thick photoresist used and the difficulty of clearing the post holes all the way down to the underlying metal. The design rules for this process are summarized in Table 2.1.

Design Rules		
Resistors	Maximum current per micron width	10 mA
	Minimum width	5 μm
	Allowance for proton straggle	1 μm
	Ohmic contact resistance	0.035±0.015 Ωmm
	N^+ layer sheet resistance	10±1.6 $\Omega/\square$
Capacitors	Maximum size	2 pF
	Top plate clearance from bottom plate edge	2 μm
Metal	Thick metal minimum line / space	2 / 3 μm
	Thin metal minimum line / space	1 / 2 μm
	Airbridge minimum line / space	5 / 5 μm
All layers	Alignment tolerance	±0.5 μm

Table 2.1: Summary of design rules for circuits fabricated using the process outlined in this chapter.

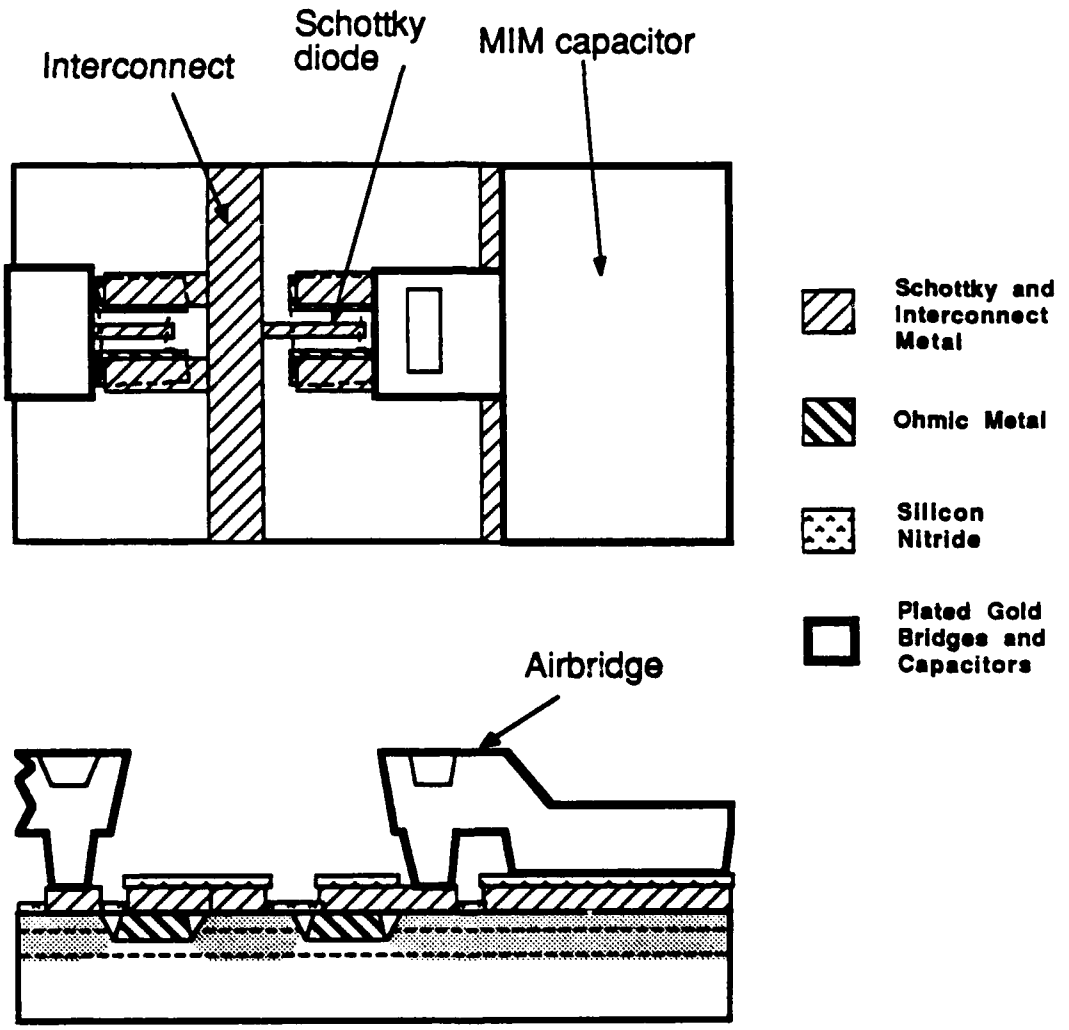


Figure 2.3: Completed airbridge and capacitor structures.

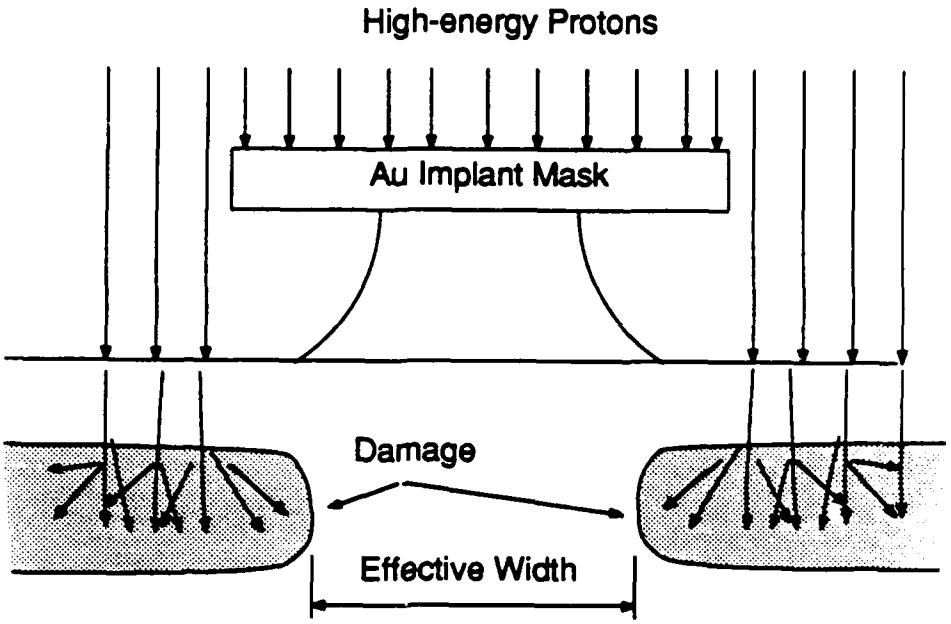


Figure 2.4: Proton straggle effect on width of active region

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Chapter 3

High-speed sampling

3.1 Introduction

Sampling has long been used as a means of measuring phenomena that occur on a time scale shorter than the response time of existing instrumentation. In electronics, possibly the earliest "sampler" was the "cycle contact maker". This instrument placed a potentiometer across a bipolar dc voltage source. The sliding contact was connected through a galvanometer to the output of an ac power generator. This contact was made for only a small fraction of every ac cycle. The sliding contact was then adjusted manually over many cycles for zero deflection of the galvanometer, at which point the generator voltage could be determined at this particular instant in its cycle by the position of the potentiometer's sliding contact. Credit for the first sampling system should probably go to H.L. Callendar [3.1] who combined the "cycle contact maker" with a "recording potentiometer" and a synchronous motor to provide automatic recording of the potentiometer position as the relative phase of the contact maker was gradually advanced. In this instrument, the galvanometer was replaced by a relay that connected a servo motor to the bipolar dc voltage source (Fig. 3.1). The servo motor automatically adjusted the sliding contact to null the voltage across the relay coil, and the contact position was automatically recorded by a pen attached to the potentiometer's sliding contact so as to trace out the generator waveform on a strip recorder. A remarkable thing about this invention is not only

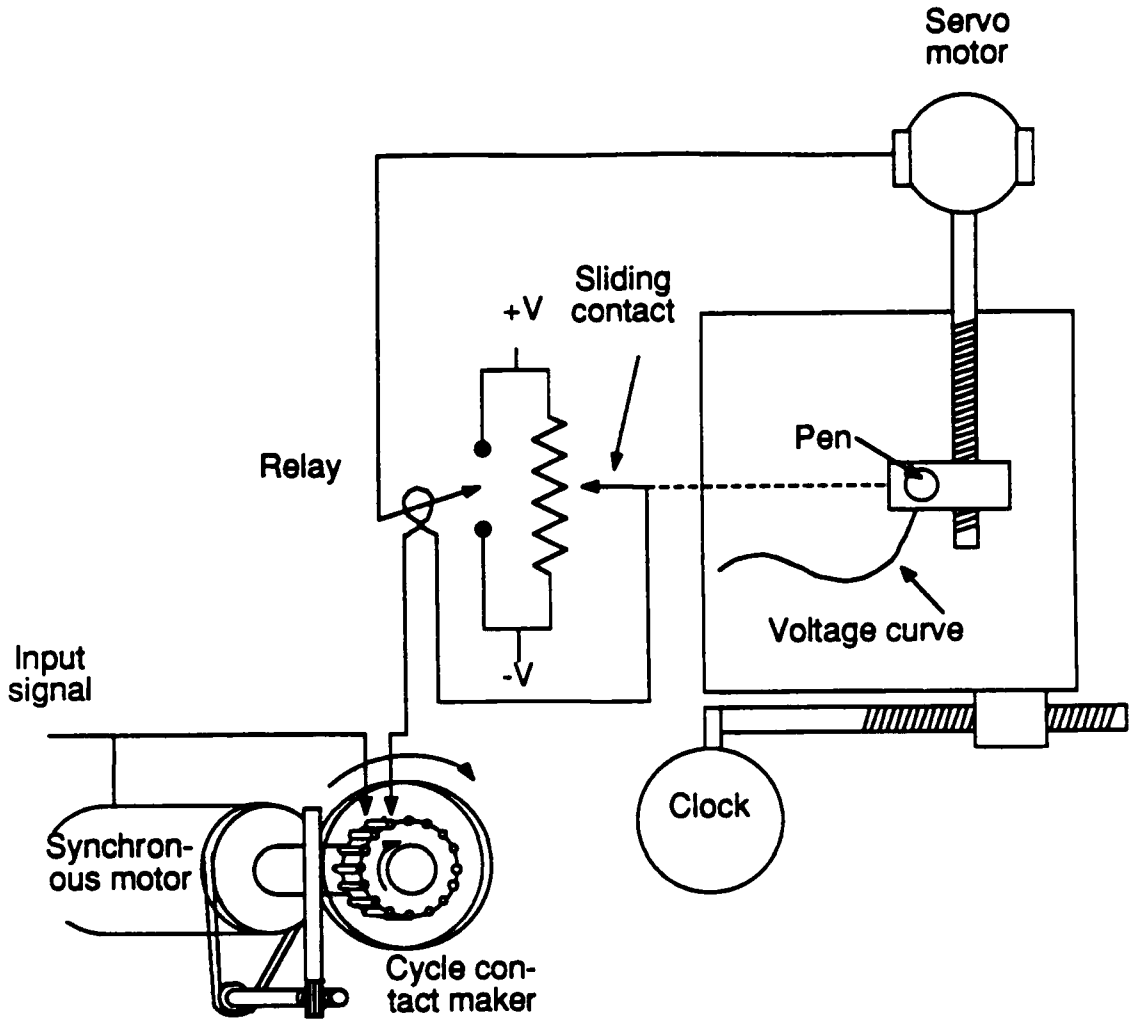

Figure 3.1: Callendar's mechanized "null-seeking" sampling system. The servo-motor adjusts the potentiometer sliding-contact position to null the voltage across the relay coil and record the instantaneous voltage with a pen connected directly to the bridge wire.

its ability to record 'high-frequency' waveforms, but also its inherent accuracy due to the null-seeking technique.

To make his "alternating cycle curve recorder" Callendar had to confront many of the same issues as today's sampling oscilloscope designer. He used the potentiometer to provide a null-seeking system that would be tolerant of the inevitable variations in contact resistance and avoid errors due to device nonlinearities and hysteresis. He realized that although contact resistance would not effect the accuracy directly, it

would "make the pen lag behind the correct reading, owing to want of quickness in responding." The quickness in responding is now called "dot-response" (response to a single sample) or "sampling efficiency." The recording drum rotation was controlled by a clock, while the phase advance was controlled by a synchronous motor which played the role of today's "time-base" and "trigger-recognizer."

Reeves [3.2] provides a history of stroboscopic sampling from the time of Callendar through the two and four diode sampling bridges and divides the various instruments into two classes: open loop (class 1) and closed loop (class 2). Reeves goes on to describe his own machine [3.3] which he claims is the first class 2 strobing oscilloscope. His work is emphasized here because it contains all of the elements and addresses most of the problems of even the most modern sampling oscilloscope. With the possible exception of random sampling [3.4] and the traveling wave bridge [3.5], contributions to this field since Reeves have involved the application of new technologies and new circuit design techniques to the basic circuits and functional blocks discussed by Reeves. The work presented in this chapter is no exception. Gallium Arsenide (GaAs) integrated circuit technology and microwave design techniques are applied to the sampling gate to produce a ten times improvement in bandwidth over the state of the art.

Although the history of the sampling gate is long, the design techniques presented in the literature are either highly qualitative or only apply for a specific signal processing technique. In addition, many major contributors to the development of high-speed sampling have either never published their work or have reported in obscure corporate publications. This is possibly because most of the 'art' of sampler design is considered proprietary by those working in the field. Grove's analysis [3.6] is quite thorough for the rf design, but does not derive the IF response. An attempt is made in the following sections to cover sampler theory at the level necessary for design.

3.2 Sampling theory

3.2.1 Qualitative discussion

A general sampling system was considered in §3.1. For a more detailed look at the sampling bridge operation, Fig. 3.2 shows the sampling bridge structure used

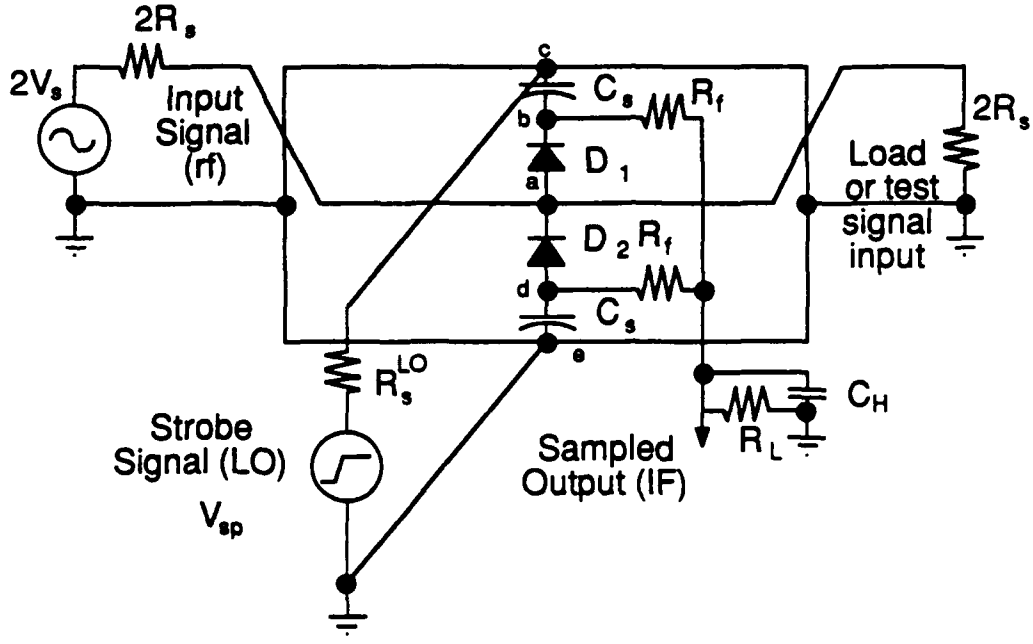

Figure 3.2: Grove's two diode sampling bridge. The signal to be sampled is input from the left and travels to the right. The sampled signal is stored on the sampling capacitors. A test signal may be brought in from the right, or the port may be terminated.

in 1966 by Grove in Hewlett-Packard's 12 GHz sampling oscilloscope [3.6]. This was the first major step of the sampling scope into the microwave regime and is illustrative of modern sampling techniques. The signal to be sampled is input from the left and travels through the sampling structure. The ground of the signal line is

split and the sampling diodes are placed across the gap in series with two coupling capacitors. The step, which is to drive the sampling diodes is applied across this split in the signal ground which acts a balanced transmission line that is shorted at both ends. This shorted transmission line differentiates the input step function so that the voltage applied across the diodes is impulse like. The pulses will also be balanced with respect to the signal line so that there is little coupling between the strobe generator line and the signal line.

If the strobe pulses are synchronous with the rf signal, the samples will always be taken at the same time, t_0, in the rf waveform. The capacitors will charge up a small amount during each sample period until node (d) charges to $-\frac{V_{sp}}{2} + V_s(t_0)$ and node (b) charges to $\frac{V_{sp}}{2} + V_s(t_C)$. The IF output into an open circuit will then be $V_s(t_0)$, where t_0 is the time of arrival of the sampling pulse. If the rf frequency is offset by a small amount from a harmonic of the pulse repetition rate, the output will trace out the rf input at the offset frequency.

3.2.2 Intermediate frequency response

For further consideration of the IF response, Grove's sampler can be represented by the circuit shown in Fig. 3.3, where the sampling diode has been replaced by an ideal switch with resistance $(R_d + R_j)/2$, which represents the parallel combination of the two sampling diodes' ohmic resistance R_d and junction resistance R_j when the diodes are 'on', R_s is the equivalent source resistance, C_H is the hold capacitance, R_L is the load resistance on the IF port, and V_s is a periodic voltage source with fundamental frequency f_{rf}. When the switch is closed, the current through the sample capacitor C_s will increase rapidly. The small filter resistance R_f isolates this high-speed waveform from the low-frequency components connected to the IF output port. Once the switch reopens, the charge on C_s will redistribute between C_s and C_H. The net effect is the same as if the two capacitors were connected in parallel, but high-frequency resonances in the IF circuitry are isolated from the high-speed switch. For the remainder of this analysis, R_f will be neglected.

Since the switch will only be closed for a small fraction of the input signal cycle, V_s can be replaced with a *piecewise constant* source V_s' which only changes value at

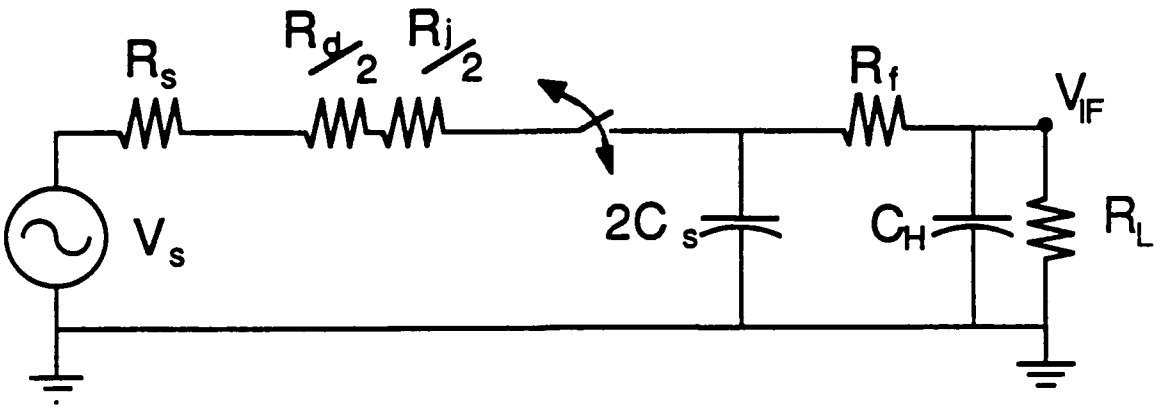

Figure 3.3: Simplified equivalent circuit of the two diode sampler.

the moment the switch is closed, t_m. So

$$V_s'(t) = \begin{cases} V_s(t) & \text{if } t = t_1, t_2 \ldots \\ V_s(int(t/\Delta t)\Delta t) & \text{otherwise} \end{cases} \tag{3.1}$$

where $int()$ means integer part and Δt is the time between switch closings. The strobe pulse repetition rate, also called the local oscillator (LO) frequency, is

$$f_{LO} = \frac{1}{\Delta t}$$

An example of an rf waveform and its piecewise constant representation is shown in Fig. 3.4. Now let the fundamental frequency component of V_s' be

$$f_{IF} = q f_{LO} - f_{rf}$$

where q is an integer, so that V_s' has a repetition rate of f_{IF}. So, assuming that f_{IF} is sufficiently small, V_s' is varying much more slowly than the sampling rate, and the circuit of Fig. 3.3 can be analyzed as a switched capacitor filter [3.7].

The output voltage, V_{IF} after the $m+1$ sample is equal to that after the mth sample plus the voltage change due to current integrated by capacitor $C_H + 2C_s$

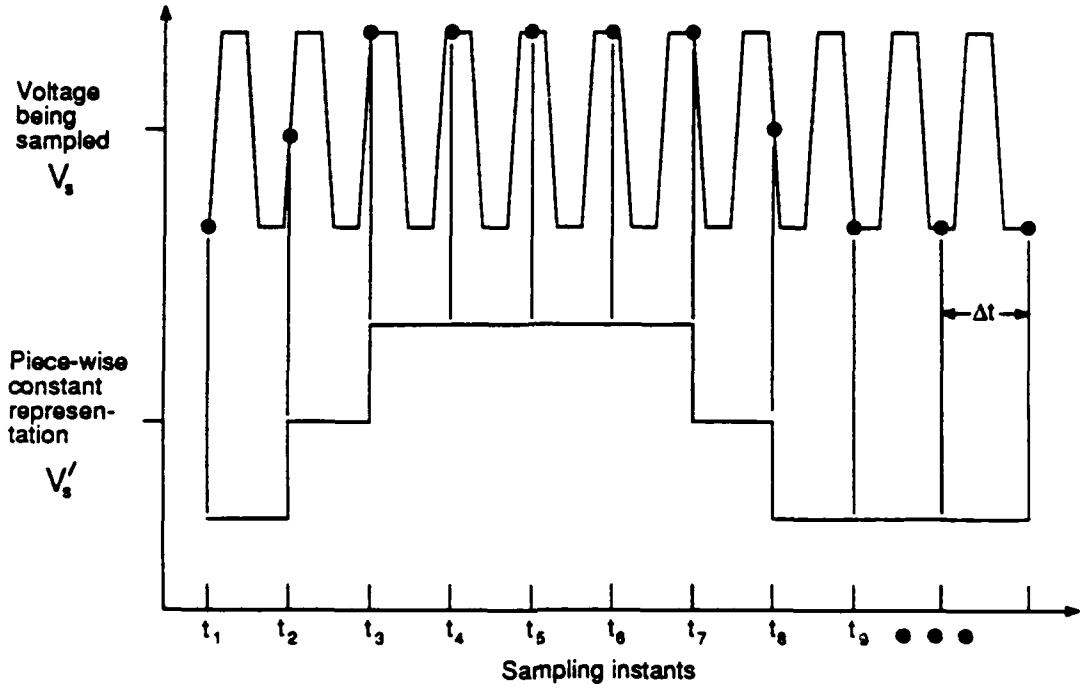

Figure 3.4: Piecewise constant sampled signal representation.

during the $m+1$ sample, minus that due to the current leaking off through resistor R_L between samples. Assuming that the sampling interval t_{on} is much less than the charging time constant τ_f,

$$t_{on} \ll \tau_f = (C_H + 2C_s)\frac{R_L(R_s + R_d/2 + R_j/2)}{R_L + R_s + R_d/2 + R_j/2}$$

and that the time between samples Δt is much less than the slow leakage time constant τ_s,

$$\Delta t \ll \tau_s = R_L(C_H + 2C_s)$$

V_{IF} after the $m+1$ sample may be written

$$V_{IF}^{(m+1)} = V_{IF}^{(m)} + \frac{t_{on}}{\tau_f}(V_s' - V_{IF}^{(m)}) - \frac{\Delta t}{\tau_s}V_{IF}^{(m)} \tag{3.2}$$

This can be solved using the z-transform to get

$$V_{IF}(z) = \frac{t_{on}/\tau_f}{1 - z^{-1}(1 - \frac{\Delta t}{\tau_s} - \frac{t_{on}}{\tau_f})} V_s'(z) \tag{3.3}$$

which has an impulse-invariant equivalent analog transfer function [3.8]

$$V_{IF}(f_{IF}) = \frac{\frac{t_{on}}{\tau_f \Delta t}}{j2\pi f_{IF} + \frac{1}{\tau_s} + \frac{t_{on}}{\tau_f \Delta t}} V_s'(f_{IF}) \tag{3.4}$$

The *voltage* conversion efficiency is therefore given by,

$$(CE)_v = \frac{\frac{t_{on}}{\tau_f \Delta t}}{\sqrt{(2\pi f_{IF})^2 + (\frac{1}{\tau_s} + \frac{t_{on}}{\tau_f \Delta t})^2}} \tag{3.5}$$

The *power* conversion efficiency is just the square of the voltage conversion efficiency multiplied by the ratio of the actual rf source and IF load impedances

$$(CE)_p = (CE)_v{}^2 \frac{2R_s}{R_L} \tag{3.6}$$

It can readily be shown that the power conversion efficiency is maximized for $R_L = (R_s + R_d/2 + R_j/2)/D$, where $D = t_{on}/\Delta t$ is the duty cycle, yielding an optimum conversion efficiency of

$$(CE)_p = \frac{1}{2} \frac{DR_s}{R_s + R_d/2 + R_j/2} \tag{3.7}$$

as if the sampler were replaced by a resistor R_{IF} as shown in Fig. 3.5a. The value of the equivalent sampler resistance at the IF frequency is given by

$$R_{IF} = \frac{(R_s + R_d/2 + R_j/2)}{D} \tag{3.8}$$

which is simply the resistance connected to the ideal switch divided by the duty cycle. That $(CE)_p$ varies *linearly* with the duty cycle, is one of the primary advantages, in some applications, of the sampler over the harmonic mixer, which has a power conversion efficiency that varies with the square of duty cycle. This simple model also gives the correct value of the IF bandwidth,

$$f_{IF(3-dB)} = \frac{1}{2\pi(R_{IF} \parallel R_L)C_H} \tag{3.9}$$

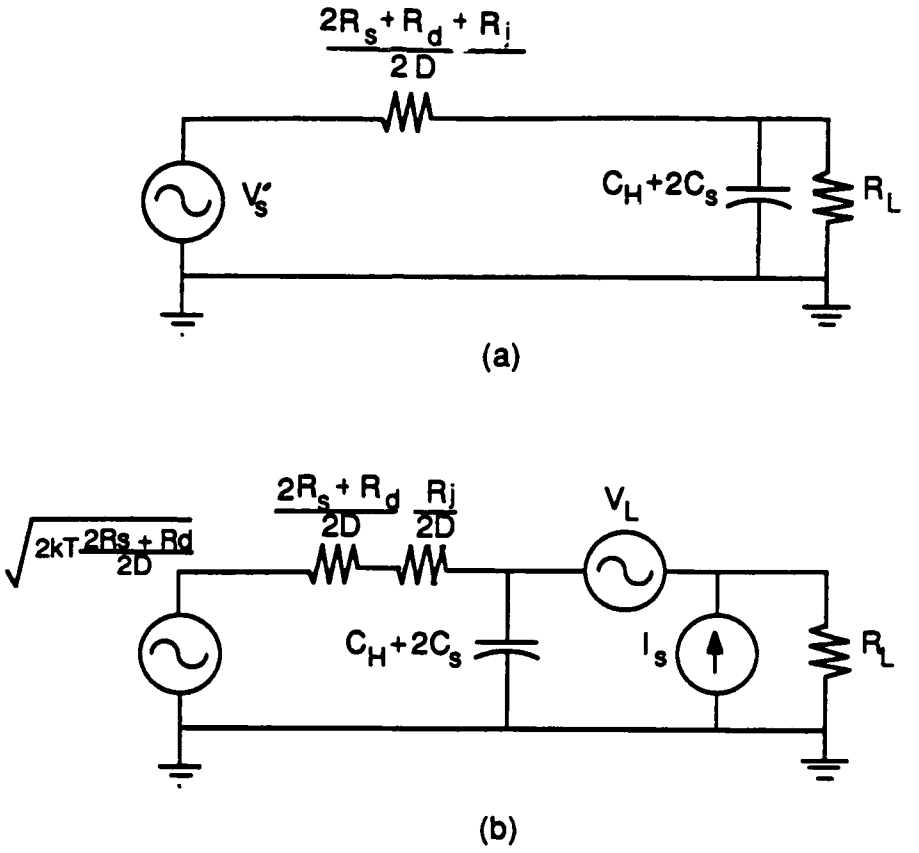

Figure 3.5: Intermediate frequency equivalent circuit (a) and noise model (b).

The thermal noise voltage of the physical resistances scales in the same manor as the resistor value, as shown in Fig. 3.5b. From this model, the input-referred mean-square voltage noise spectral density is determined to be

$$v_n^2 = \frac{2k_BT}{D}(R_s + R_d/2) + v_L^2 + (I_sR_L)^2 \tag{3.10}$$

where k_B is the Boltzmann constant and T is absolute temperature. Here, v_L is the input noise voltage of the IF load, which may not be a physical resistor, and I_s is the diode shot noise current. Using this model, it can readily be determined that the noise figure of the sampler is approximately equal to its power conversion loss if shot noise is neglected.

3.2.3 Input frequency limitations

In §3.2.2, the IF response was not a function of the input frequency so long as Δt could be chosen to give the desired f_{IF}. However, the input frequency – also called radio frequency input (rf) – is restricted by several major factors. The lower limit will be set by the longest Δt that can be attained. The upper limit is a function of t_{on} and sampling device parasitics. If t_{on} is not much less than an input signal period, V_s can not be replaced by a piecewise constant source as in §3.2.2. In this case, the time dependant conductance of the switch must be multiplied by the input signal to obtain the capacitor charging current. At each sample, the switch conductance will be multiplying a slightly different portion of the input waveform so that the integrated current on the capacitor is proportional to the *convolution* of the switch conductance and the input signal voltage. The switch conductance waveform can therefore be considered the impulse response of the system. For a square shaped aperture the transfer function is $sin(\pi f t_{on})/\pi f t_{on}$ so the 3-dB bandwidth is, $f^{(1)}_{rf(3-dB)} = 0.44/t_{on}$. However, the widely used rule of thumb, $f^{(1)}_{rf(3-dB)} = 0.35/t_{on}$ [3.6] provides a more conservative estimate.

While IF response can be discussed in general terms, the rf bandwidth is dependant on the particularly implementation. The samplers discussed here are all of the two diode variety briefly outlined in §3.2.1. When a diode replaces the ideal switch, as in Fig. 3.6, capacitance and series resistance prevent in two ways the sampler from attaining the bandwidth made possible by the strobe pulse. First, the capacitive loading of the shunt diodes on the rf line causes rf voltage at the diodes to have a pole in its frequency response at $f^{(2)}_{rf(3-dB)} = 1/(4\pi C_{j0}(R_s + R_d/2))$, where C_{j0} is the zero-bias junction capacitance. Secondly, the diode capacitance broadens the strobe pulsewidth applied to the diodes by introducing a pole in the LO transfer function at $f_{LO(3-dB)} = 1/\pi R_{se} C_{j0}$. From Fig. 3.6, the equivalent resistance in series with the diodes is $R_{se} = 2R_d + (R^{LO}_s Z_e)/(R^{LO}_s + Z_e)$, where Z_e is the impedance of the even mode on the rf transmission line, and R^{LO}_s is the LO source impedance.

To determine the rf bandwidth due to all the factors discussed above, it is first necessary to determine the effect of the pole in the LO transfer function on the rf transfer function. This is handled in a quasi-empirical manner by assuming that t_{on}

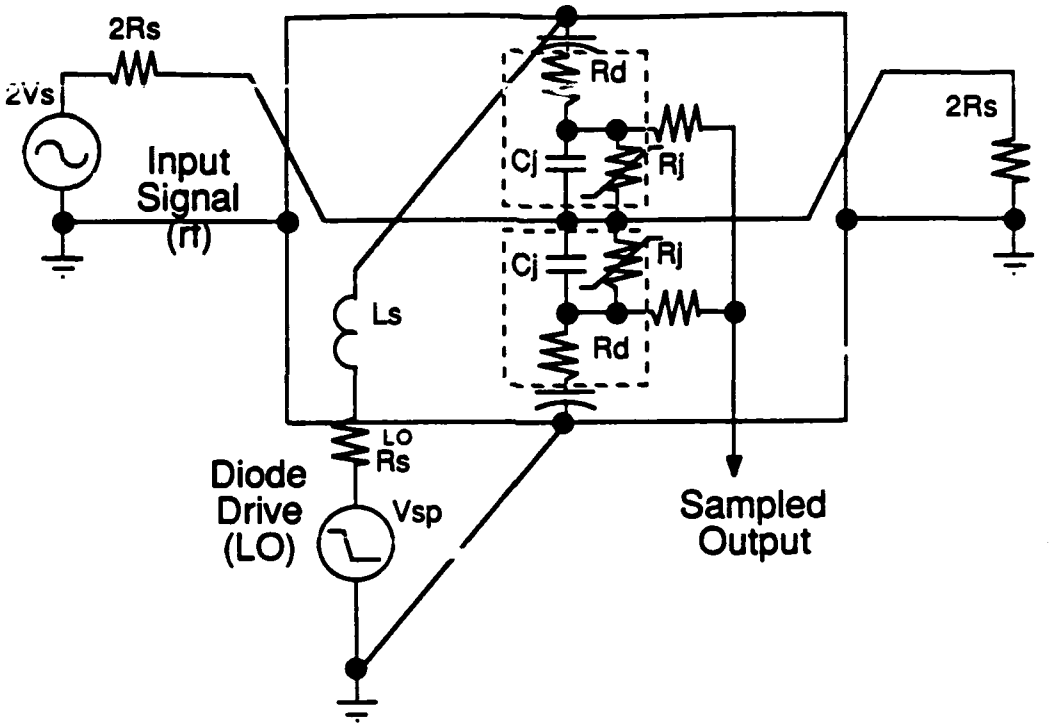

Figure 3.6: Sampler equivalent circuit including diode parasitics.

is one half the actual voltage pulse width. That this could be the case is illustrated in Fig. 3.7. Obviously, by adjusting the diode bias, t_{on} may be varied without changing the voltage pulse. However, in a typical system, the range of adjustment is limited since too little reverse bias will result in unwanted diode switching due to LO pulse ringing, and too much reverse bias will degrade the conversion efficiency of the sampler. So, under typical conditions, if the LO input pulse is known, the broadened pulse can be computed from the LO transfer function. One half of the broadened pulse width is then taken as t_{on}. Now, by using the root-sum-squared (RSS) technique [3.9], the various factors can be combined to produce an estimate of the rf bandwidth:

$$f_{rf(3-dB)} = \frac{1}{2\pi\sqrt{(2C_{j0}(R_s + R_d))^2 + (R_{se}C_{j0}/4)^2 + (PW/2)^2}} \tag{3.11}$$

Here, PW is the sampling voltage pulse width in the absence of parasitics, which is approximately equal to the fall time of the strobe signal generator.

Inductive parasitics in the fully monolithic samplers discussed later are on the order of a few picohenrys. While this is not totally negligible, it is small enough to

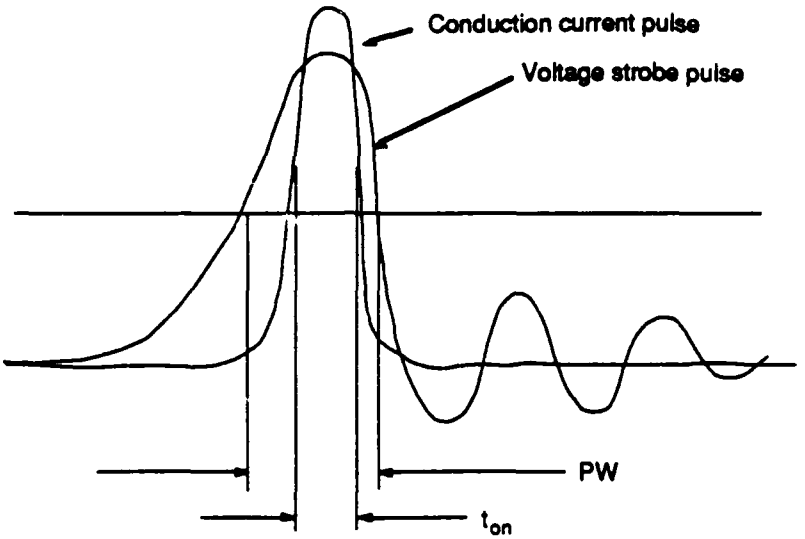

Figure 3.7: Relationship between sampling aperture, defined by the conduction current pulse, and voltage strobe pulse width. The aperture, t_{on} is typically one half of the strobe pulse width, PW.

ignore for this simple analysis. In samplers which require hybrid assembly, inductive parasitics can be one of the primary design constraints. Even the modern beam-leaded diode can have parasitic inductance greater than $\sim 100pH$ [3.10]. Grove [3.6] presents an analysis which includes inductive effects and provides the following design equations:

$$f_n = \frac{1}{2\pi\sqrt{LC}}, \quad \delta = \frac{R_d/2+R_s}{2}\sqrt{\frac{C}{L}} \tag{3.12}$$

where f_n is the rf cutoff frequency, L is the diode package inductance divided by two, C is two times the diode junction capacitance, and δ is the damping factor. These equations must be used when designing a monolithic sampler to be certain that inductance is not becoming a significant factor. Also, in a monolithic sampler, inductance may be added to reduce the damping factor and increase the bandwidth.

The analysis of the preceding sections presented the following elements which must be considered for maximum rf bandwidth:

- Sampling diode capacitance and series resistance
- Inductive and other parasitics associated with layout and interconnections
- Falltime of the strobe signal generator.

The nonlinear transmission line described in §1.2.2 provides a ten times improvement in slew rate over the step recovery diode while maintaining similar amplitude. Because the NLTL is implemented in monolithic GaAs IC technology, it can be integrated with the sampling head to drastically reduce the inductance normally associated with the connection between the sampler and the strobe signal generator. Thus, the NLTL in conjunction with a low-parasitic monolithic sampler provides the possibility of dramatic improvements in rf bandwidth. Several designs of such a sampling system are presented in the following sections.

3.3 Monolithic samplers

3.3.1 Generation I

Design and layout

The objective of the first monolithic sampler design was to demonstrate the superior performance afforded by the NLTL, with minimum risk. To accomplish this objective, the sampler was designed around a proven NLTL design [3.11]. Choosing the same epitaxial layer doping and thickness allowed use of measured diode and resistor properties which are highly reproducible using molecular beam epitaxy (MBE). The two diode sampling bridge was selected because of its simplicity. The problem with this structure is that, even in more modern implementations [3.12,13], it is highly three dimensional and requires hybrid assembly. By using coplanar waveguide for the transmission lines,it can be collapsed into one plane, so that it can be monolithically integrated with a NLTL strobe signal generator [3.14].

The design of Fig. 3.8 reduces the structure to one plane by using the even and odd modes of CPW [3.15], allowing monolithic integration of the entire sampling

head. The design is similar to that reported by Hunton [3.16] for a 4 GHz double balanced mixer. The major improvement of this design is that it minimizes the use of slotline which is lossy and dispersive. In addition, monolithic integration and the use a NLTL strobe pulse generator provide a much greater bandwidth. The RF signal to be sampled is applied to the port labeled "External signal input" and travels in the normal (odd) mode on the vertical CPW. NLTLs drive the ports labeled "Strobe pulse input", and "Internal test signal input". Only the final sections of the on-chip NLTLs are shown in the figure. The NLTL design is identical to that reported in [3.11]. The sawtooth wave applied to the "Strobe pulse input" of Fig. 3.8 travels in the odd mode on the horizontal CPW until it is applied to the sampling diodes and the slotline (even) mode of the RF CPW. The even mode is shorted by airbridge connections 180 μm from the sampling diodes. The reflected wave turns the diodes off after a round trip time of $\sim$4 ps. An additional NLTL is located below the sampling head to provide a high speed test signal to evaluate the sampler risetime. Beyond the diodes, the ground planes were taken back to a 130 μm spacing to increase the impedance of the even CPW mode, while maintaining 50Ω for the odd mode.

The central portion of the sampler has a CPW ground-to-ground spacing just large enough to accommodate the two sampling diodes. In this first design, Schottky metal was the same as the (thick) interconnect metal, so, using the design rules of Chapter 2, the minimum spacing was 3 μm . In the layout of Fig. 3.9 the two diodes required 45 μm. This is the distance the center conductor of the strobe line must protrude to make connection to the opposite ground plane. The inductance of this protrusion can be estimated to be 28 pH from

$$L = 2 \times 10^{-4} l \left[\ln\left(\frac{l}{w+t}\right) + 1.19 + 0.22\frac{w+t}{l} \right] \tag{3.13}$$

where L is in nH, $l = 45$, $t = 1.4$, and $w = 5$ are the length, thickness, and width of the strip in microns [3.17]. It would be preferable to choose the diode junction capacitance such that when two are driven in series, $R_{se}C \geq L/R_{se}$, where R_{se} is given in §3.2.3 and C is half the diode junction capacitance. In this case the design would not depend critically on the exact value of L.

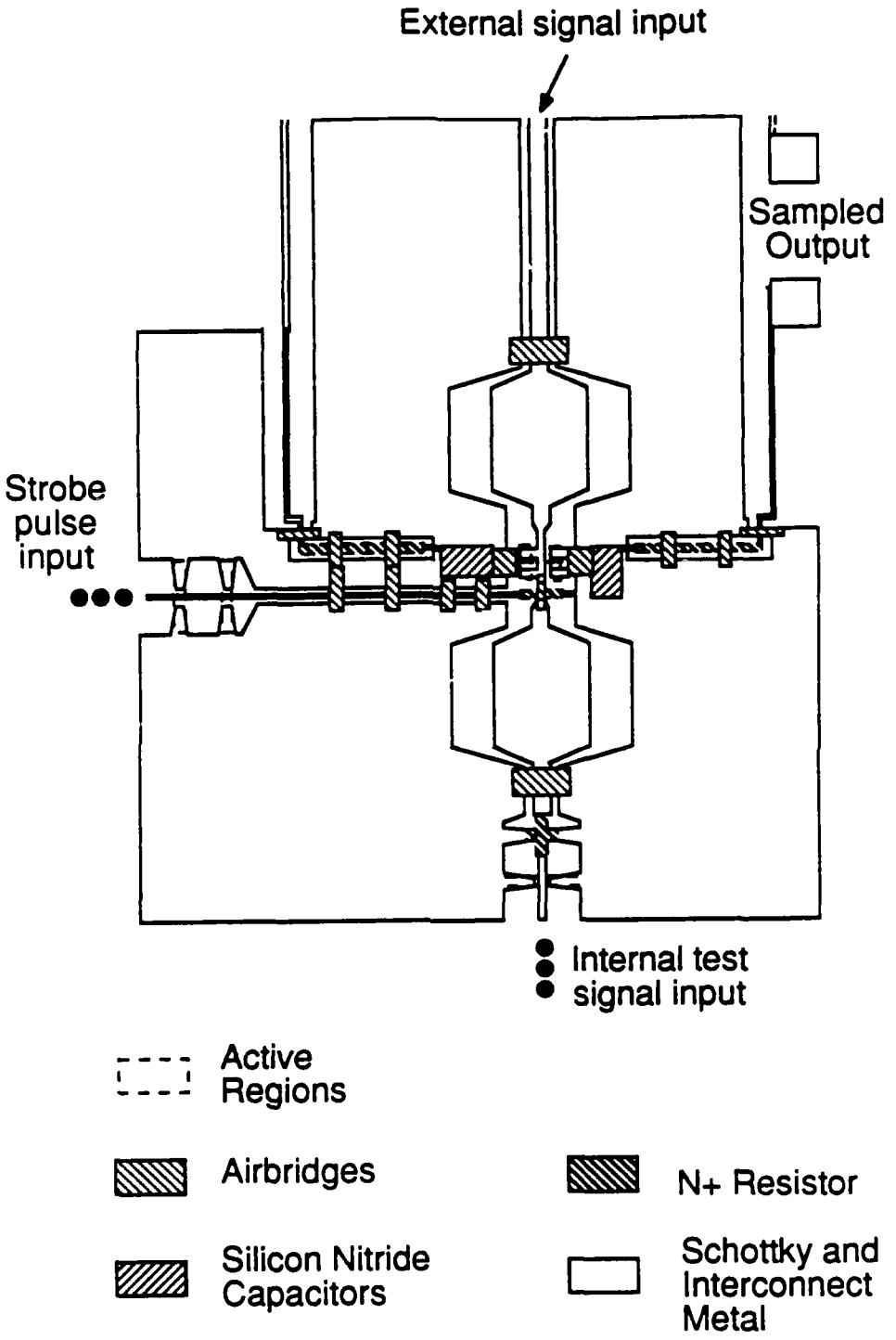

Figure 3.8: Layout of Generation I sampler showing the sampler and portions of two nonlinear transmission lines.

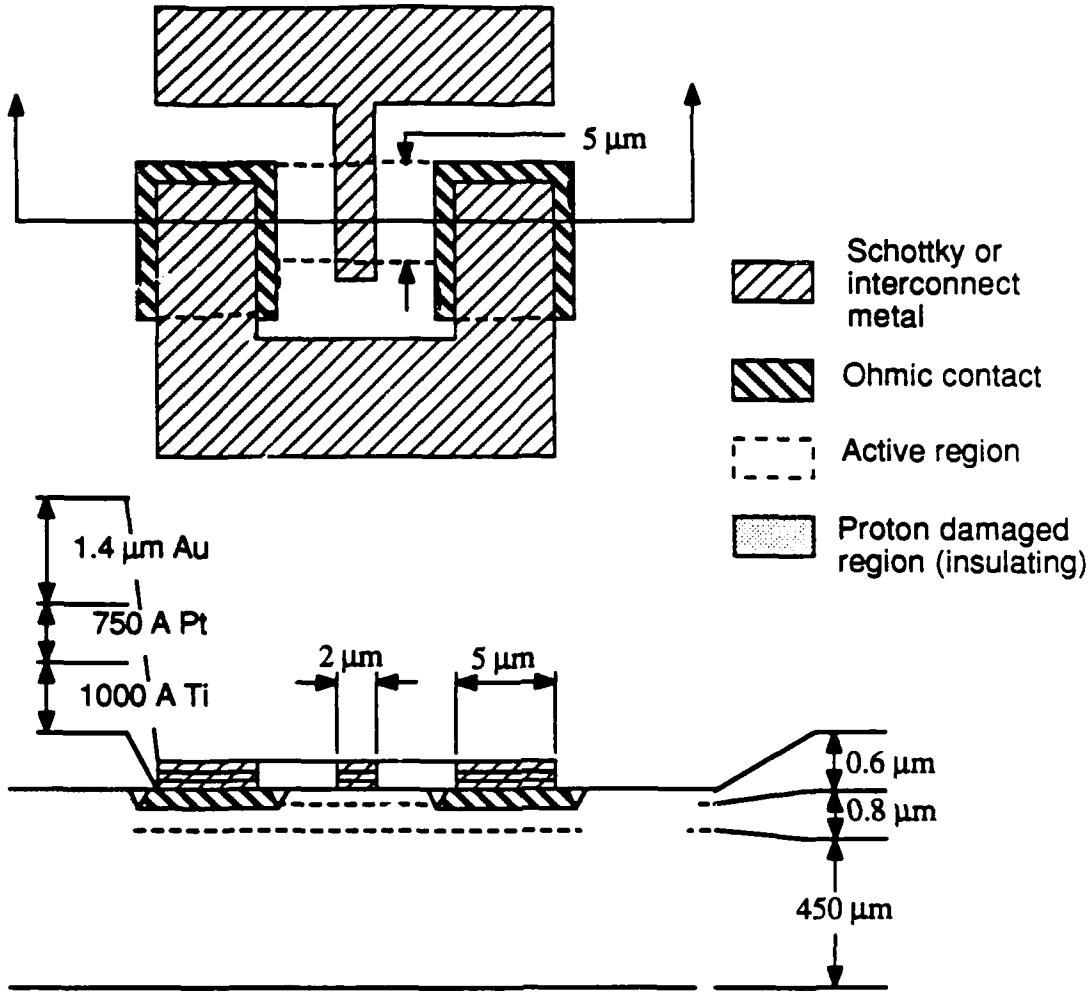

Figure 3.9: Diode layout for the Generation I sampler. The Schottky contact extends beyond the active region so that alignment error does not change area of the diode.

The actual value of the diode junction capacitance was chosen so that the diode conduction current was larger than the displacement current of the junction capacitance. This is desirable because the sampling diodes are also varactors. That is, there will be mixing due to both nonlinear resistance and capacitance. Since the nonlinear capacitor current is maximum where the slope of the diode strobe pulse is maximum, the capacitive sampling function is more broad than the resistive and has a double peak. Since the relative contributions of the two nonlinear processes are related the respective currents, the ratio of the diode conduction current to the peak junction capacitor current should be maximized. For a diode forward conduction

current of 5 mA and a strobe pulse slew rate of 7.1×10^{11}V/s, the diode capacitance should be less than 7 fF. The value chosen was 6 fF, which is a 2×5 μm diode on the 3×10^{16} doped N^- layer. Diodes smaller than this were judged impractical because of excessive N^- resistance.

Assuming 2 fF of stray capacitance in addition to the 6 fF junction capacitance and a diode series resistance of 60Ω, the damping factor of the sampling loop, which includes the two sampling diodes in series and the inductance of the connection, is 0.9. With this damping factor, the bandwidth predicted with the simple RC model of §3.2.3 is pessimistic by a factor of 2. Using the RC model in this case gives substantial room for error in the calculated sampling-loop bandwidth of 250 GHz.

The NLTL used as a strobe pulse generator (also called the local oscillator or LO) produces a 2.5 V, 3.5 ps falltime sawtooth wave when driven with an 8 GHz, 23 dBm sine wave. Since the slope of the rising edge is negligible in comparison with that of the falling edge, the derivative of the waveform is a 3.5 ps impulse, full-width at half-maximum (FWHM). Used as a strobe pulse generator, this can give $\sim$ 1.8 ps sampling bridge aperture times if the diode bias is set at $\sim$50% of the impulse magnitude.

When the strobe is applied to the CPW even mode and the sampling diodes, voltage will be divided across the strobe source impedance and the CPW even mode impedance. To achieve maximum voltage across the sampling diodes, the even mode impedance should be maximized. Using scale models on Stycast[1] material, it was determined that the largest even mode CPW impedance that could be obtained without introducing excessive parasitics to the odd mode was 75Ω. Driving the even mode from the center of the transmission line reduces the impedance by two. So, in this design, $Z_e = 75\Omega/2$, $Z_s = 90\Omega$, $r_s = 60\Omega$, and $C_{j0} = 8fF$, giving the sampling loop a time constant of 0.6 ps. Using root-sum-squares (RSS) convolution, the predicted strobe pulse width is, $\sqrt{3.5^2 + 0.6^2} = 3.6$ ps, giving an aperture time of 1.8 ps. The pole in the RF circuit will contribute 1.9 ps to the system risetime, so the total system will have a risetime of $\sqrt{1.8^2 + 1.9^2} = 2.6$ ps and a corresponding 3 dB bandwidth of 130 GHz.

[1]Stycast is a trademark of Emerson & Cuming

The relative contributions of the various parasitics to the system time constant discussed above are summarized in Fig. 3.10. The 3.5 ps strobe fall time and the 0.6 ps time constant of the sampling loop are divided by two since the resulting sampling aperture is approximately one half of the parasitic-broadened strobe pulse (see Fig. 3.7). Note that strobe parasitics are negligible in comparison with the diode loading on the rf line (rf pole).

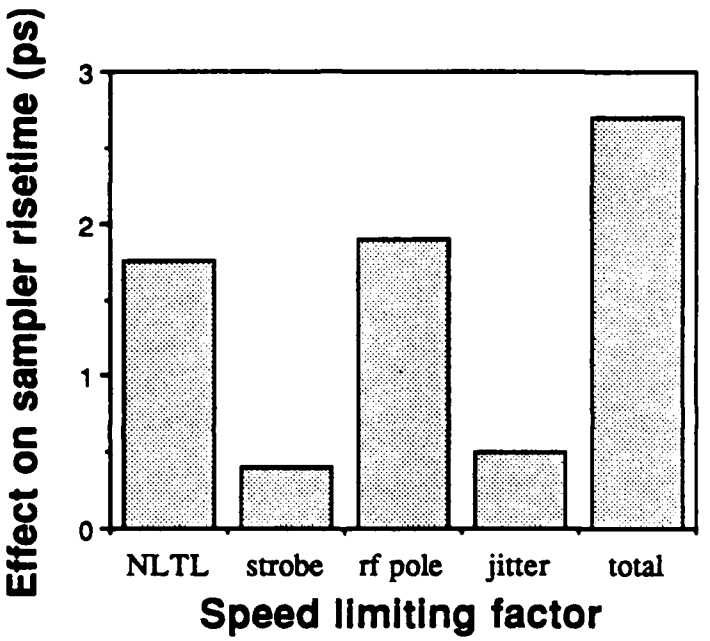

Figure 3.10: Risetime limiting factors of the Generation I sampler. Column 1 is the NLTL output falltime divided by two, which is the diode aperture time in the absence of parasitics. Column 2 represents the contribution the sampling diodes loading the strobe circuit while Column 3 shows their effect on the rf circuit. Timing jitter is depicted in Column 4 and the RSS total is shown in Column 5.

Results

The sampler bandwidth was evaluated by probing internal nodes of the circuit using direct electrooptic sampling and by using the sampling circuit to measure the output of both the NLTL internal test signal generator and an external 80–128 GHz

frequency multiplier. A strobe pulse width of 4.0 ps was measured using direct electrooptic sampling (Fig. 3.11). From RSS deconvolution of the 1.9 ps electrooptic

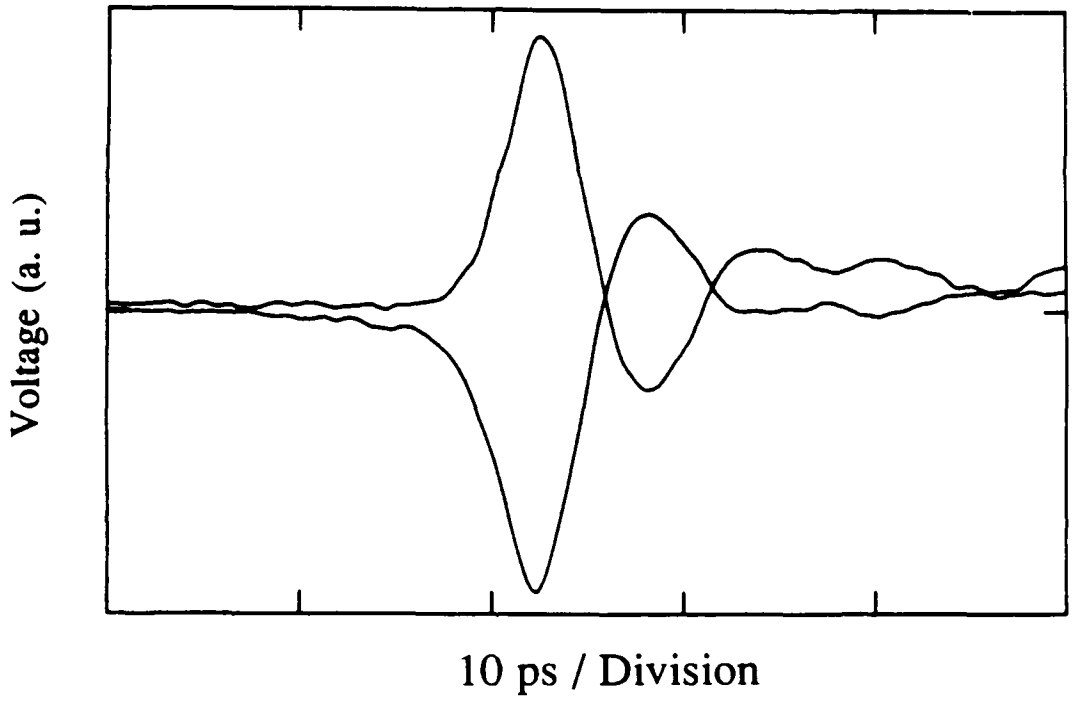

Figure 3.11: Electrooptically sampled Generation I sampler strobe pulses. The positive going waveform is the voltage strobe pulse appearing at the anode of D_2; the negative going pulse is at the cathode of D_1.

measurement system impulse response, the strobe pulse width is $\sim$ 3.5 ps FWHM. Depending on the diode bias, the corresponding diode sampler aperture time is between 1.8 and 3.5 ps.

The test signal generator, identical to the LO strobe pulse generator, is a NLTL whose output is attenuated 50:1. Measured by electrooptic sampling, the test signal has a falltime of approximately 3.5 ps. The test signal 10%–90% falltime measured by the diode sampling head was 4.0 ps (Fig. 3.12). Using RSS deconvolution, the sampling circuit is found to have a 2.7 ps 10%–90% risetime, with a corresponding

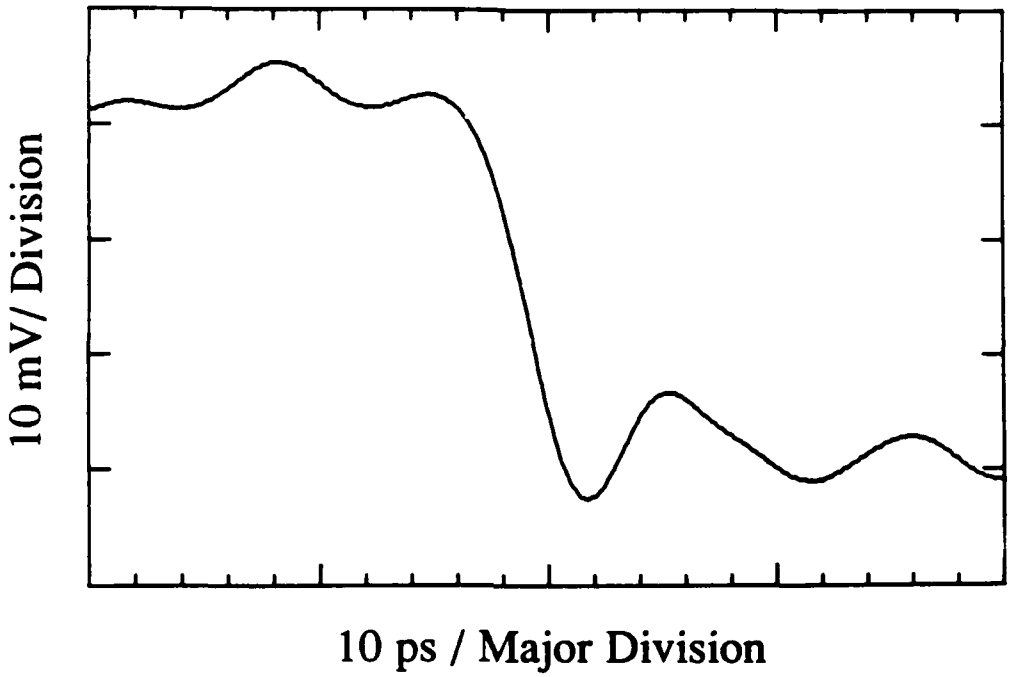

Figure 3.12: Sampled output of a 50:1 attenuated nonlinear transmission line. The measured falltime is 4.0 ps; the actual falltime is estimated to be 3.5 ps.

bandwidth of roughly 130 GHz.

To get a better measure of the speed of this sampler, a 5 times frequency multiplier probe, which has measurable power from 80 to 128 GHz [3.18], was used. With the multiplier probe providing the input test signal, the node being electrically sampled was simultaneously probed by the electrooptic sampler (see Fig. 3.13). The power computed from the voltage measured by the sampling head was divided by that measured with the optical probe. The result is shown in Fig. 3.14, where 0 dB corresponds to the video response at 82 MHz. The graph shows that the response is relatively flat up to 128 GHz. If the phase were linear up to this frequency, the time resolution of this all electrical sampler would be better than 2.7 ps. However, as this measurement is normalized to the node being sampled, it does not include

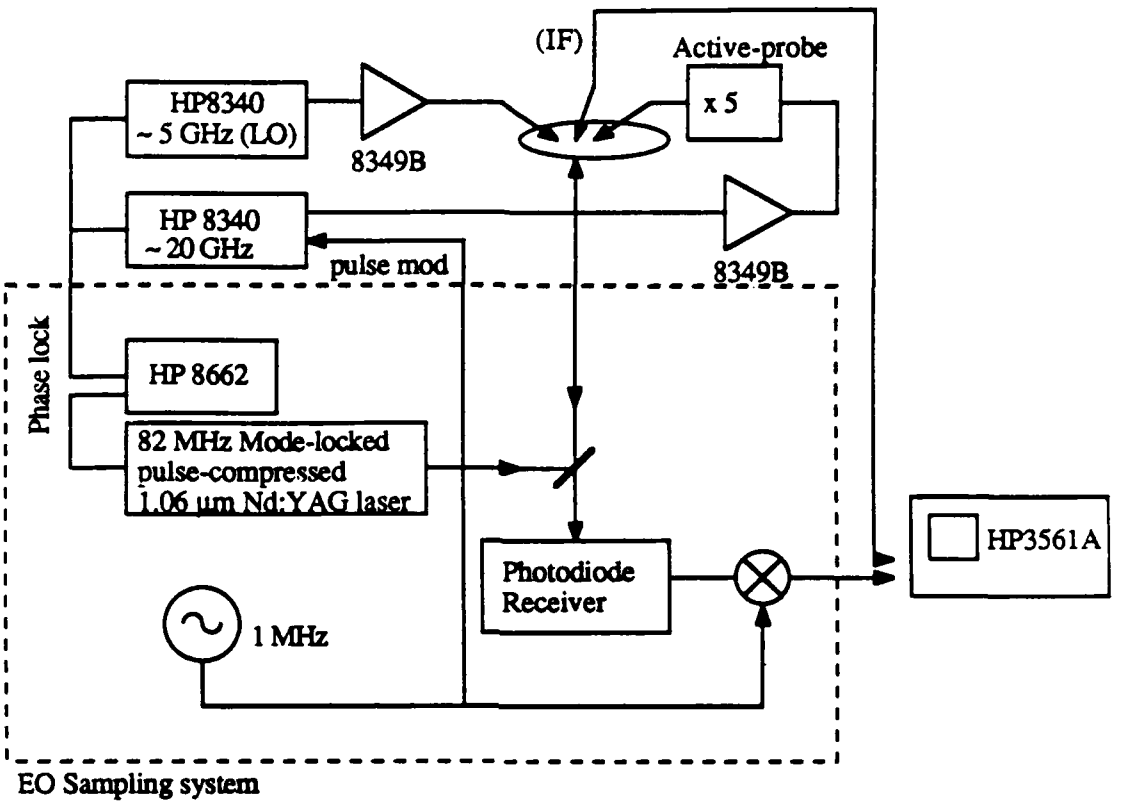

Figure 3.13: Experimental set-up for measuring sampler response.

the effect of the rf pole.

Depending on the LO drive power, the 1 dB compression point was as high as 10 dBm. The equivalent input noise voltage was 90 nV/$\sqrt{Hz}$. At 5 GHz, RF to IF isolation was 55 dB, LO to IF isolation 63 dB, and the LO to RF isolation was 68 dB [3.19].

3.3.2 Generation II

Design and layout

The motivation behind development of the second generation sampler was to produce more samplers that could be used in various applications, not necessarily to improve the design. However, to increase the number of samplers that could fit on

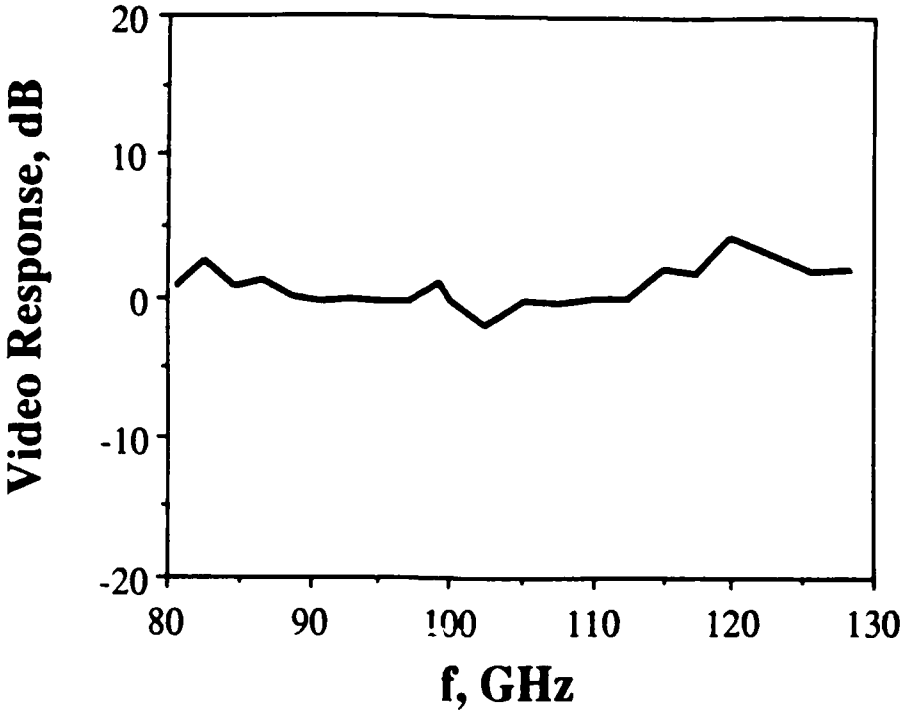

Figure 3.14: Sampler video response from 80 to 128 GHz. To obtain the video response, the sampler measured power was divided by that measured by EO sampling at the node being electrically sampled.

the wafer, it was necessary to design a more compact NLTL. This is readily accomplished by using coplanar-strip (CPS) for the interconnecting transmission lines rather than coplanar-waveguide (CPW) with its large ground planes. Unfortunately, CPS is a balanced transmission line and therefore a new sampler had to be designed which could be driven from a balanced line. Still, no changes were made to the epitaxial layer structure.

The CPS nonlinear transmission line is shown in Fig. 3.15. It is nearly electrically equivalent to the CPW NLTL used in the previous design. The major difference is that a 90Ω CPS can have a smaller transverse dimension and lower ohmic losses. Also, the varactor diodes must be rotated 90°. This creates some difficulty since now the length of the ohmic is parallel to the transmission line rather than the width. It is usually desirable to make the ohmic at least 20 μm long to minimize its resistance per unit width. If the varactor ohmics were made 20 μm long, the total length of the discontinuity presented to the transmission line would be greater

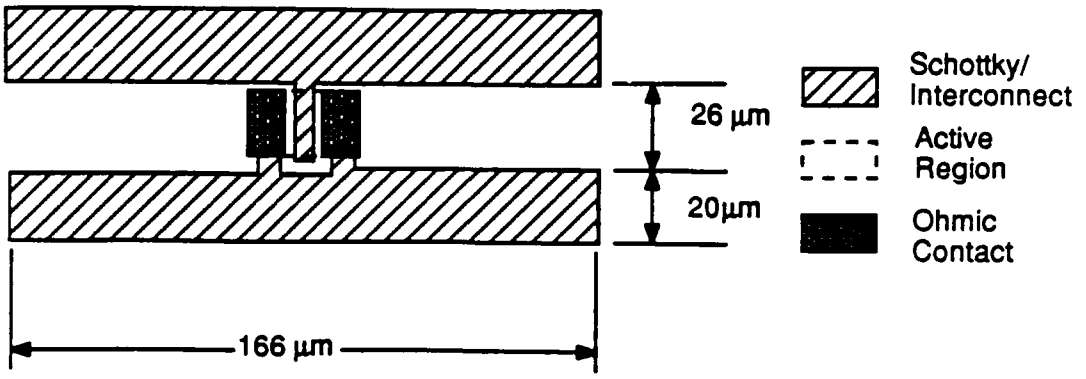

Figure 3.15: Coplanar strip (CPS) nonlinear transmission line.

than 45 μm (two ohmics and a 5 μm Schottky contact) which is over twice that in the CPW design. For this reason, the ohmics were made only 10 μm long and the consequent increase in varactor series resistance was suffered.

The sampler designed for the CPS NLTL is shown in Fig. 3.16. It is considerably simpler than the previous design since the strobe is already balanced. It is only necessary to apply the strobe to the sampling diodes in a fashion that provides a low inductance connection and isolation from the rf port. This sampler is not a feed-through sampler as in the previous design so it is not possible to provide self-test capability by adding a second NLTL. This reduces the die area substantially but makes testing much more difficult.

Results

Because of the lack of an internal test signal generator in this design, it is necessary to bring in an external test signal and use electrooptic sampling to determine the actual voltage. This is also made difficult by the CPS geometry since the small ground plane area on wafer does not suppress signals that that may be on the ground plane of the test signal probe. This is in fact the case with the frequency

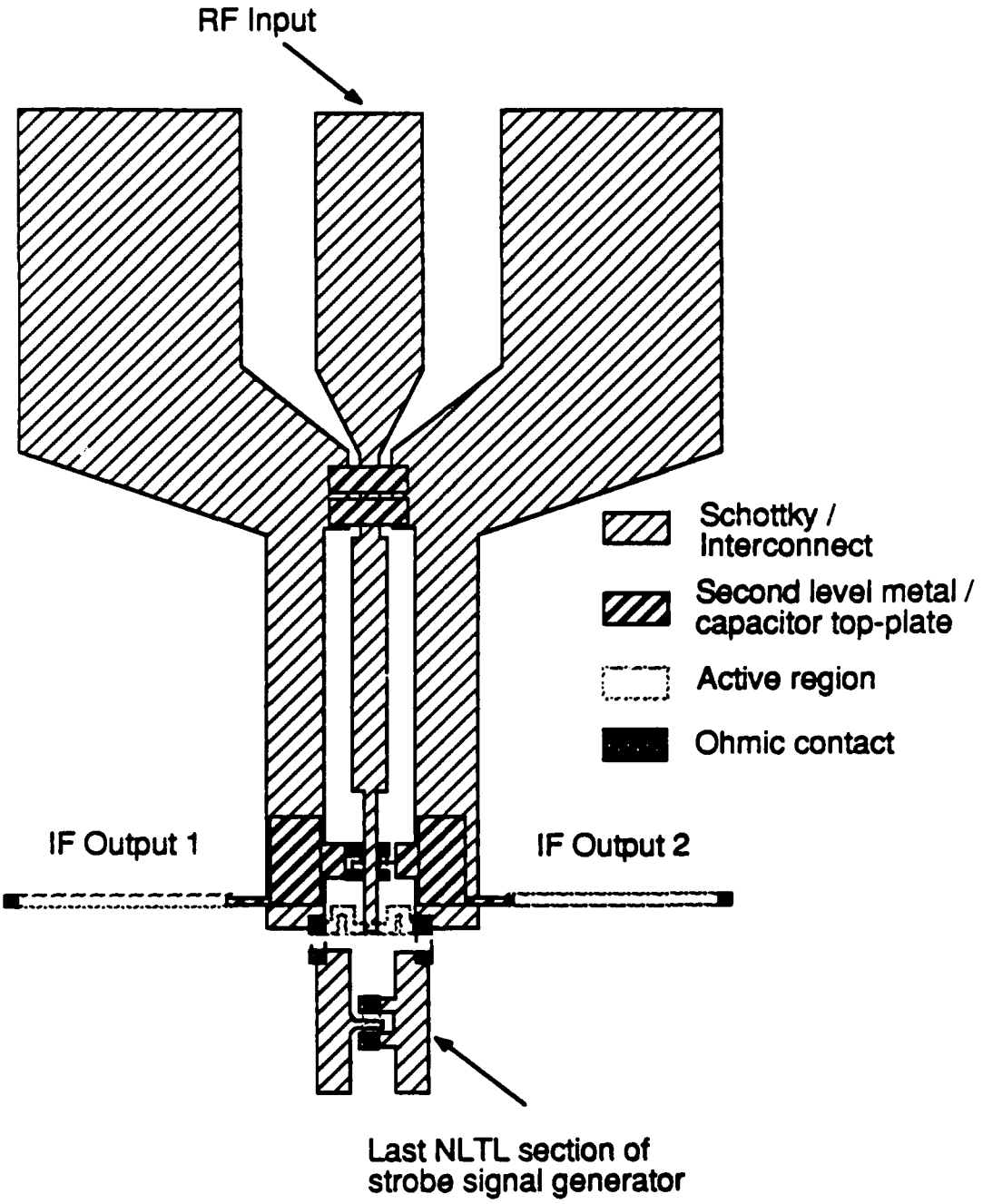

Figure 3.16: Sampler designed for the CPS NLTL.

multiplier probe used to test the previous design. This is a problem since the sampler only measures the voltage between the center conductor and ground while the EO sampler measures absolute voltage. Therefore, it is necessary to EO sample the voltage on the center conductor and subtract the the EO sampled voltage on the ground to obtain a value that can be compared with the electrically sampled result. Because these two voltages are similar in magnitude, the error involved in this measurement can be very large. Although an absolute reference could not be established, the power measured with this sampler at 100 GHz compared favorably with that measured with the previous design.

Given the problems mentioned above, on-wafer tests were abandoned and instead the performance of a packaged sampler was evaluated. This was simplified by the 'in-line' design which made the CPS sampler chip nearly a 'drop-in' replacement for the sampler used in the 40 GHz Wiltron 360 [3.20] vector network analyzer. A hybrid power splitter/balun was designed by Jay Banwait of Wiltron Company to allow two CPS NLTLs to be driven from the same coaxial connector. The two sampler dies were mounted with the power splitter and two CPW tapers for the rf ports in the Wiltron sampler package. The completed package could then be plugged directly into the IF buffer amplifier used in the Wiltron 360 network analyzer. The experimental test set-up is shown in Fig. 3.17. The conversion loss of this sampler when driven with a 500 MHz local oscillator strobe signal from a step recovery diode is shown in Fig. 3.18. The displayed conversion loss includes the 6 dB conversion loss of the second-IF mixer, the 32 dB attenuation of the first-IF monitor port, and the 39 dB gain of the buffer amplifier. The conversion loss is high because the Wiltron buffer amplifier has an input impedance of approximately 12kΩ while the sampler has an IF output impedance of $\frac{2ns}{1.8ps}(25+30) = 64k\Omega$. This gives a 16dB loss due to the voltage divider, 10 dB higher than the matched condition. The conversion loss for a matched IF is 37 dB according to Eq. (3.7). The rf test signal was provided by a Hewlett-Packard (HP) 8340A synthesizer with a frequency doubler and tripler to reach 60 GHz. The sampler measured power was normalized to that measured with a frequency-extended HP 8566B spectrum analyzer.

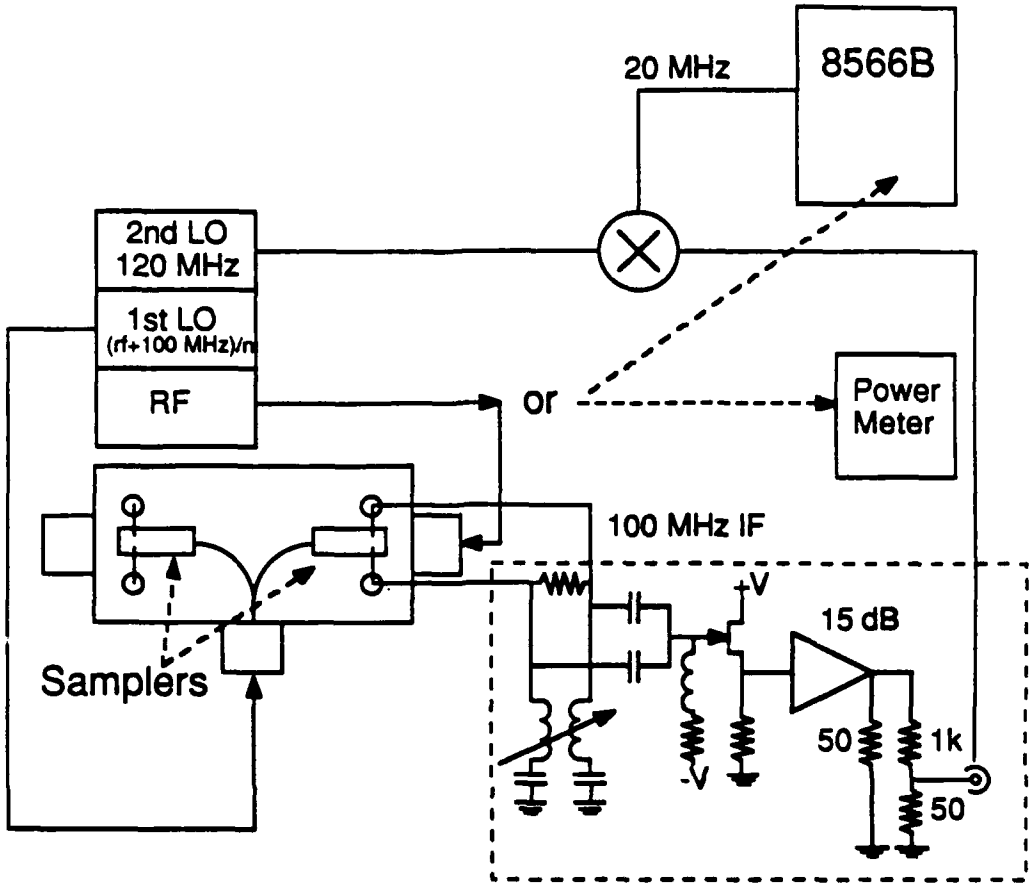

Figure 3.17: Experimental set-up for conversion loss measurement of the packaged Generation II sampler.

3.3.3 Generation III

Design and layout

The goal of the third generation sampler was to achieve the greatest bandwidth possible. Improvements were made to the NLTL, the sampling diodes, and layout. To avoid conflict between the changes to the NLTL and sampler, most of the NLTL was placed on a separate chip. This chip used a hyperabrupt doping profile as described previously [3.21] to achieve a 6 V, 1.6 ps transition. A small NLTL was placed on chip with the sampler since the output of the NLTL chip was limited to about 5 ps by the interconnecting bond wires. The sampling diode series resistance

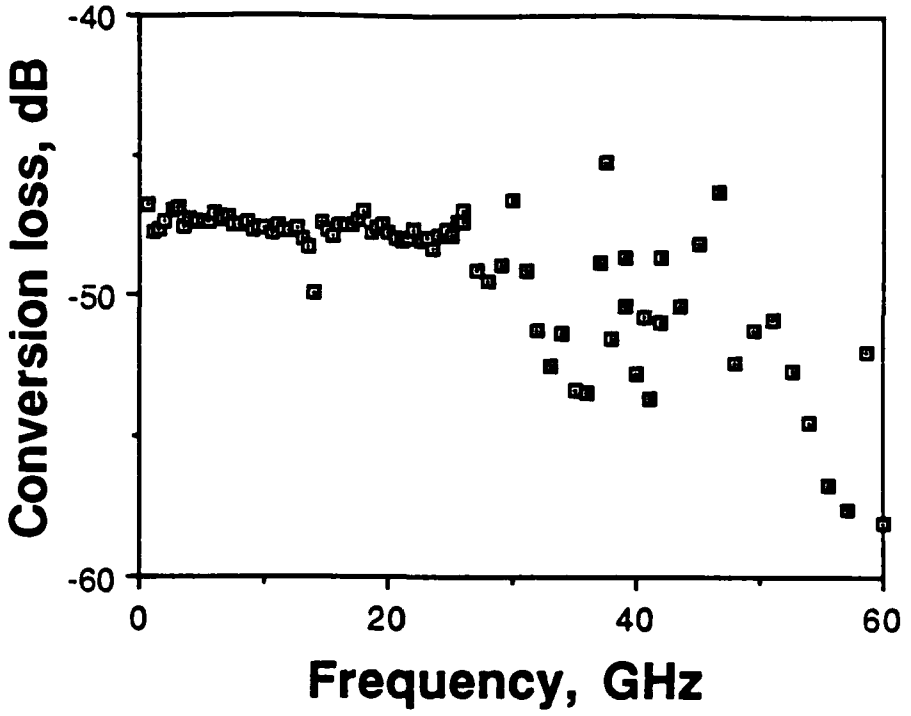

Figure 3.18: Conversion loss of the packaged CPS sampler with a 500 MHz LO using the Wiltron IF buffer amplifier.

was reduced to 12.5Ω by using an N^- layer half as thick, 0.3 μm, with 4 times the doping, $1.2 \times 10^{17}/cm^3$ while maintaining the zero bias junction capacitance, C_{j0} near 9.5 fF. The cut off frequency of the on-chip NLTL diodes was also improved by widening the ohmic contacts and bringing the ohmic metal closer to the Schottky contact to reduce series resistance. A scanning electron micrograph (SEM) of a completed NLTL diode is shown in Fig. 3.19.

Layout is perhaps the most important consideration in designing a high-speed sampler. In this design, the NLTL drives the two ground planes of the rf CPW (Fig. 3.20). To minimize the inductance of this connection, the ground planes must be close together. However, the sampling diodes must be placed between these ground planes to reduce the inductance of their connection. These conflicting goals are met by imbedding the sampling diodes into the ground planes so that only the portion of the diode which is not at zero rf potential protrudes. This reduces the length of the sampling diode connection to 8 μm . To improve yield and provide a better input match, airbridge crossovers were avoided in the rf center conductor and diode

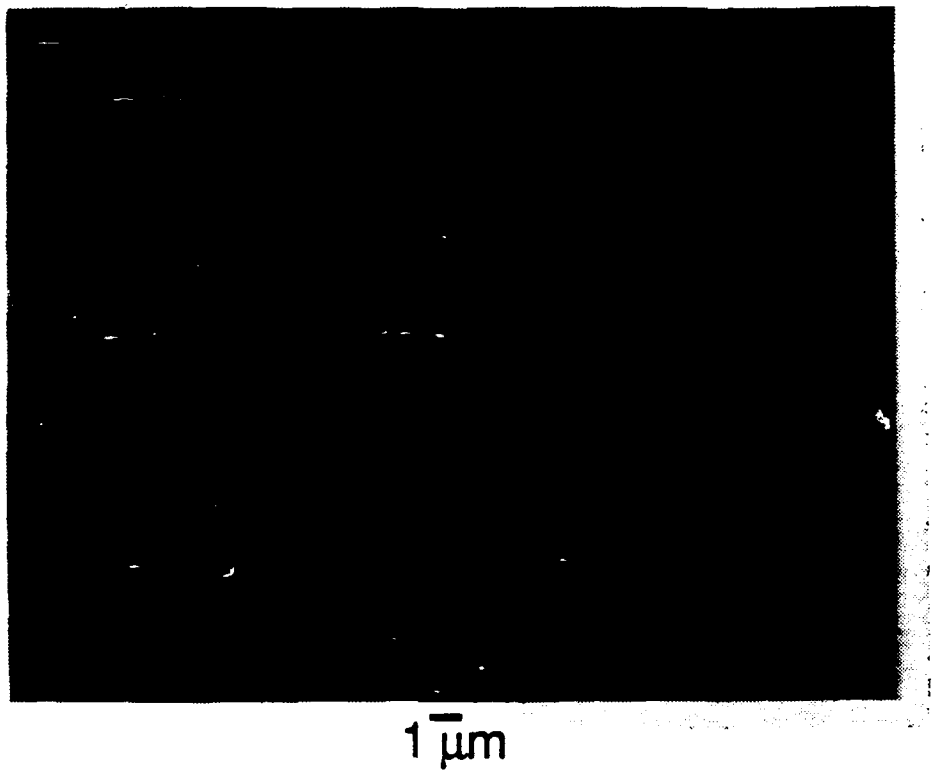

Figure 3.19: Scanning electron micrograph of an on-chip NLTL diode. Ohmic metal is brought within 1 μm of the Schottky contact.

connection and instead were used in the ground plane where many could be placed in parallel (Fig. 3.21).

Results

The speed of the sampler was evaluated by using the on-board NLTL test signal generator and by direct electrooptic sampling. With the test NLTL driven at 10 GHz + 100 Hz and the strobe NLTL driven at 5 GHz, the sampled output showed a 160 μs 90% to 10% fall-time, which corresponds to 1.6 ps in real-time (Fig. 3.22). This is the fastest transition ever measured by an all electronic device. The strobe pulses driving the sampling diodes had an estimated width of 1.7 ps after deconvolving the impulse response of the electrooptic sampler (Fig. 3.23) . The diodes were only

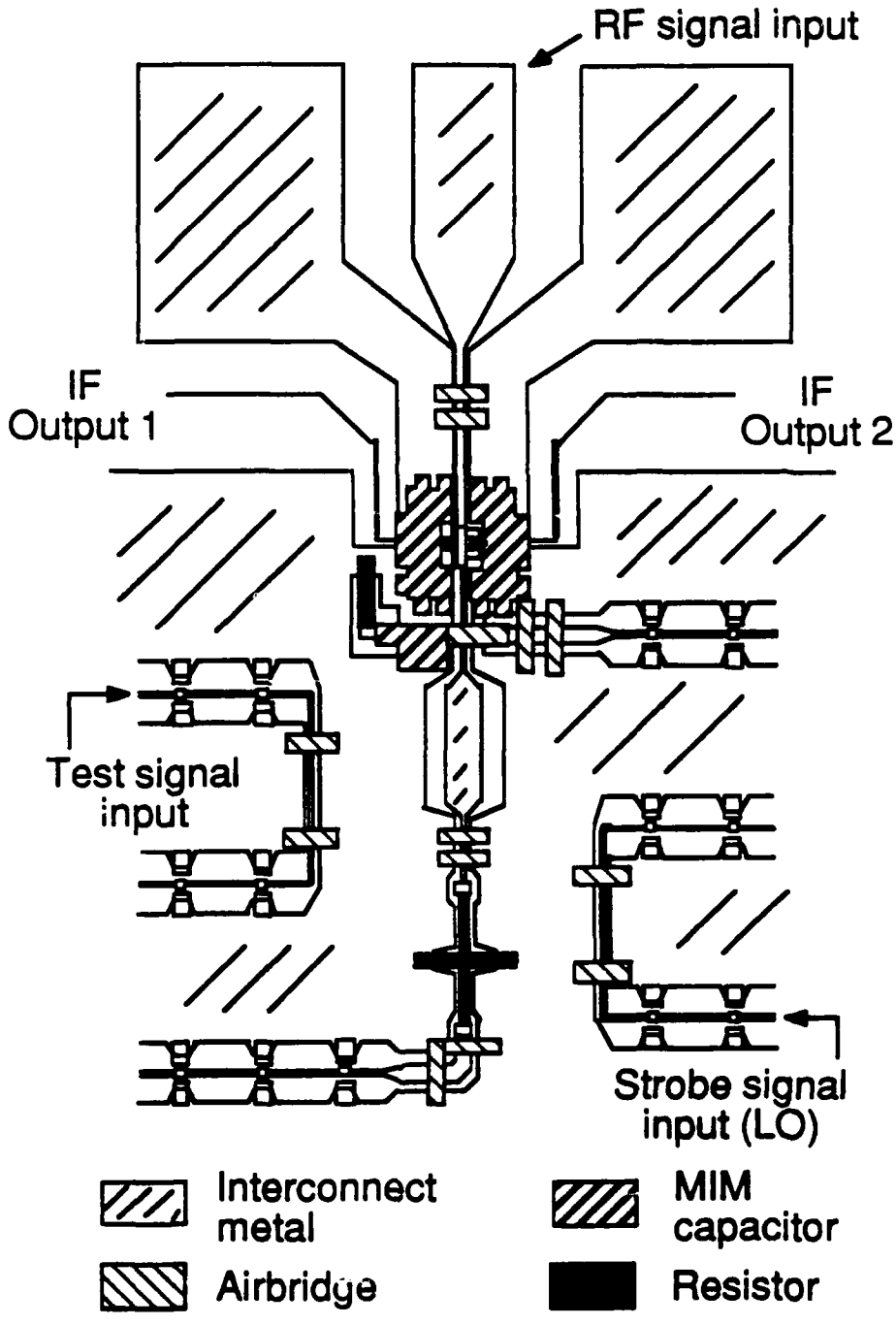

Figure 3.20: Generation III sampler layout.

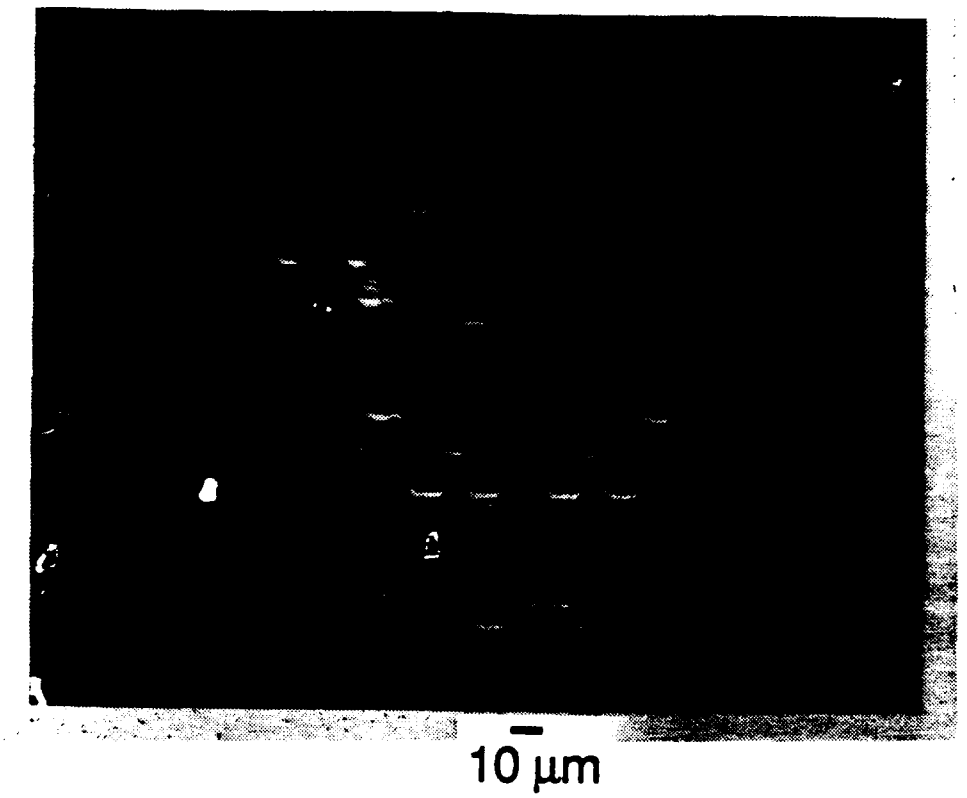

Figure 3.21: Scanning electron micrograph of the completed sampler

on for half of this time, 0.8 ps, as determined from the IF output impedance. The risetime limiting factors are summarized in Fig. 3.24 and compared with those of Generation I, Generation II being essentially the same as Generation I. The input-referred noise voltage was $0.6\mu V/\sqrt{Hz}$. The 1 dB compression point was -1 dBm. The rise-time of the sampler is estimated at 1.2 ps, which corresponds to a 290 GHz 3 dB bandwidth.

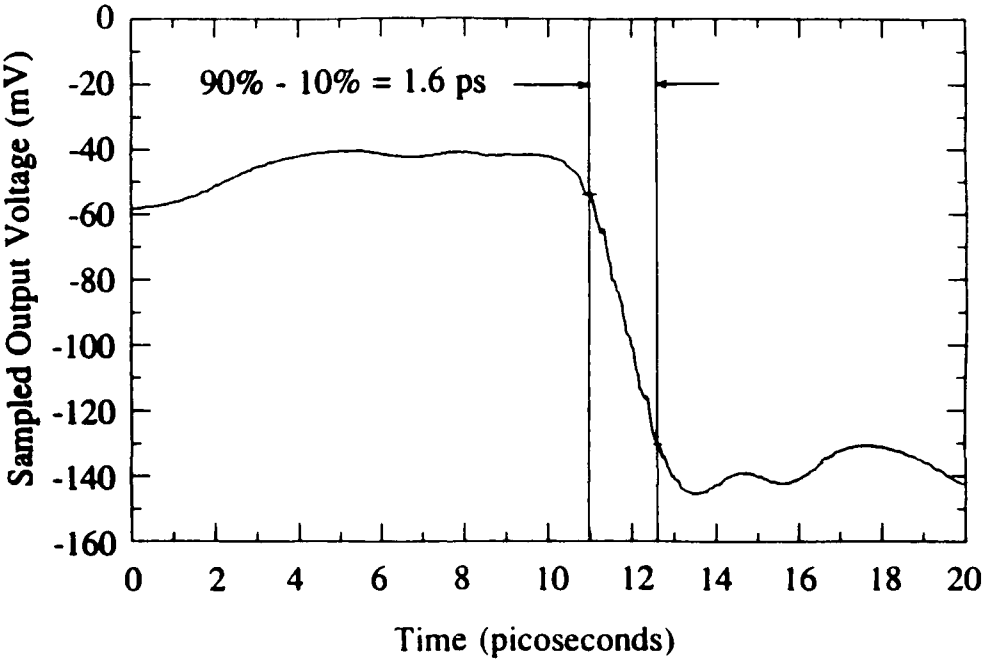

Figure 3.22: Sampled output of the 10:1 attenuated nonlinear transmission line. The measured falltime is 1.6 ps; the actual falltime is estimated to be 1.1 ps.

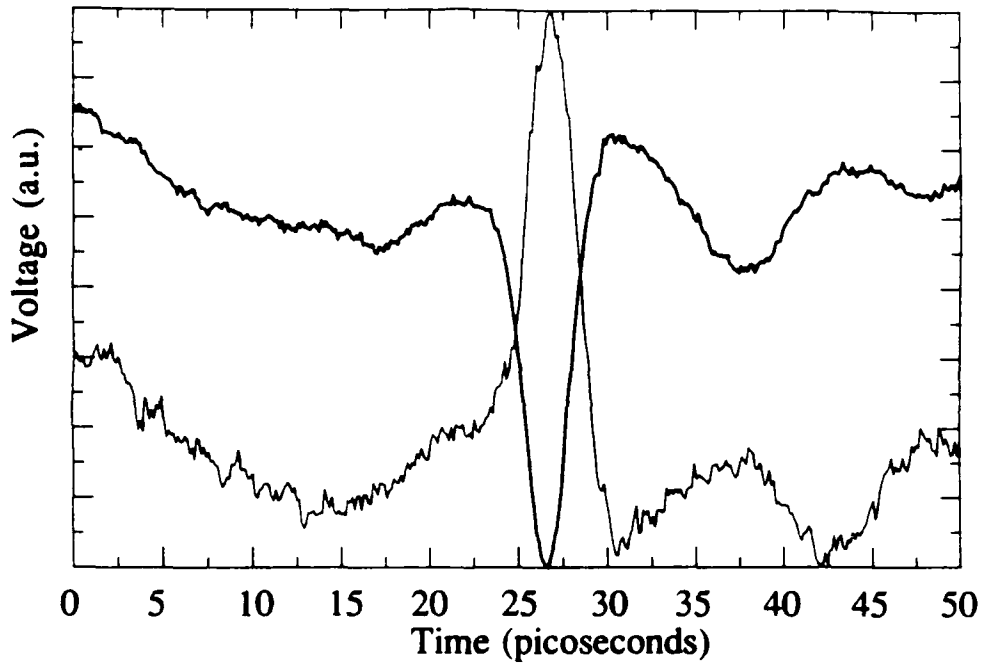

Figure 3.23: Electrooptically sampled Generation III sampler strobe pulses. The positive going waveform is the voltage strobe pulse appearing at the anode of D_2; the negative going pulse is at the cathode of D_1.

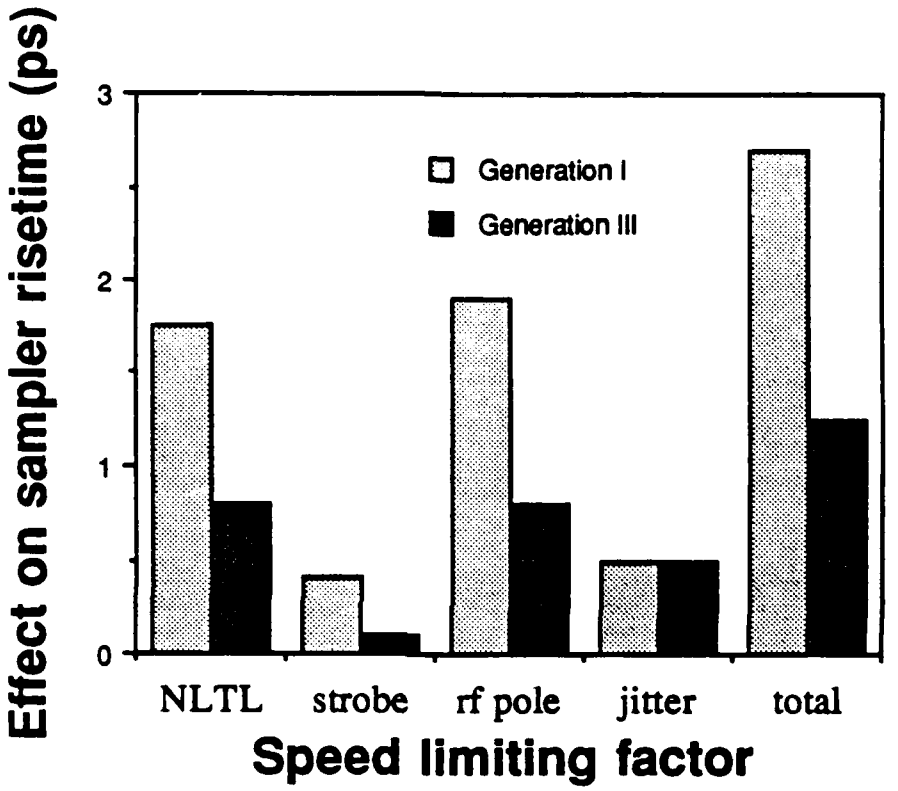

Figure 3.24: Comparison of risetime limiting factors. Column 1 is the NLTL output falltime divided by two which is diode aperture time in the absence of parasitics. Column 2 represents the contribution the sampling diodes loading the strobe circuit while Column 3 shows their effect on the rf circuit. Timing jitter is depicted in Column 4 and the RSS total is shown in Column 5.

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Chapter 4

S-parameter test-set on a chip

4.1 Introduction

To make S-parameter measurements, more is required than just a fast sampler; it is also necessary to separate the forward and reverse traveling waves. There are two methods which are widely used for the separation. One method takes advantage of the directionality provided by coupled transmission lines [4.1]. The second method, shown in Fig. 4.1, uses the directionality provided by the Wheatstone or directional bridge. The first method, being fully distributed, has the potential for higher frequency operation. However, it is exceedingly difficult to simultaneously achieve high directivity (greater than 20 dB) and ultra-broad bandwidth (greater than 3 decades). For example Krytar [4.2] offers a directional coupler with 20 dB directivity from 2 to 8 GHz, but the directivity degrades to 16 dB when the frequency range is extended to 1 to 20 GHz and degrades further to 10 dB when extended to cover the 1 to 40 GHz range. Wiltron Company [4.3] uses directional couplers in their 60 GHz network analyzer but, again, the directivity is only 10 dB. The bridge method could conceivably work at all frequencies, provided the resistors and interconnections could be made relatively parasitic free. The limitations of this technique are imposed by the voltage meter across the middle of the bridge. An improved version of this technique which uses a floating sampler is presented in the following sections. The floating sampler samples the voltage between two nodes

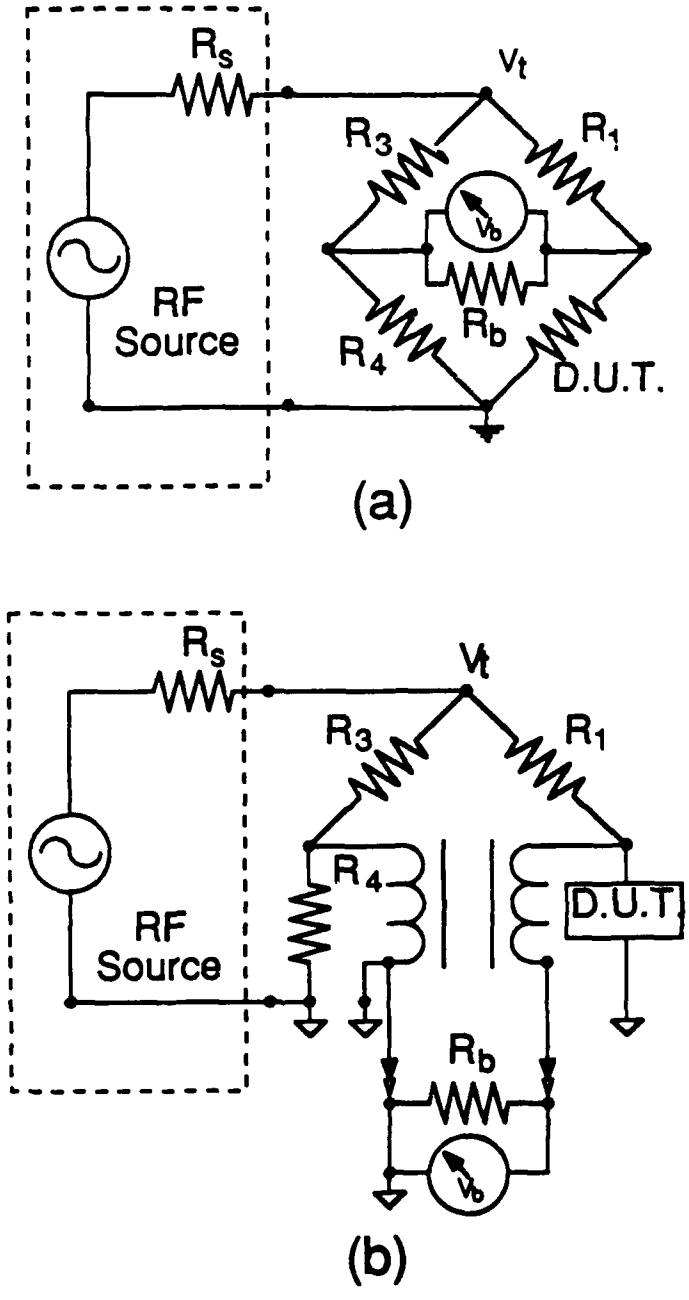

Figure 4.1: Directional bridge with (a) floating sampler and (b) single-ended sampler and balun.

where, contrary to previous practice, neither of the nodes need be grounded.

4.2 Directional sampler theory

The resistor bridge of 4.1a known as the Wheatstone or directional bridge, is balanced when [4.4]

$$R_4 R_1 = R_3 Z_d \tag{4.1}$$

where R_1, R_3, and R_4 can be complex impedances but in this case are chosen to be real. The impedance of the device under test or D.U.T., Z_d, is generally complex. The bridge is designed so that Eq. (4.1) holds when $Z_d = R_0$, where R_0 is the reference impedance, often chosen to be 50Ω. Under these conditions, the bridge output voltage V_b will be equal to zero when the impedance of the device under test equals the reference impedance. This property is useful for measuring impedance levels very close to R_0. As Z_d approaches R_0, the voltage V_b becomes proportional to the amplitude of the reflected wave from Z_d. When all the resistors are set to R_0,

$$V_b = \frac{V_s}{8}\left(\frac{Z_d - R_0}{Z_d + R_0}\right) \tag{4.2}$$

which is directly proportional to the reflection coefficient, Γ_d for all Z_d [4.5].

The difficulty is measuring the magnitude and phase of the floating voltage at high-frequencies. Usually, the voltage across the bridge is measured by using a balun to convert the voltage difference to a voltage referenced to ground, as shown in Fig. 4.1b [4.6]. However, the floating sampler presented here makes the balun superfluous. The floating sampler samples the voltage between two nodes where neither of the nodes need be grounded.

The single-ended sampler operation described in Chapter 3 measures a voltage with respect to ground because nodes (e) and (c) are at zero rf potential. Now suppose that another source V_2 is connected to nodes (c) and (e) as in Fig. 4.2, where V_1 corresponds to the original source. Now, since the impedance looking into the normally off diodes is high, the voltage at node (a) is V_1, the voltage at node (b) is $V_2 + V_{SP}/2 + V_{c1}$, and the voltage at node (d) is $V_2 - V_{SP}/2 + V_{c2}$, where $V_{c1,2}$ is the dc voltage on capacitors $C_{1,2}$. Setting the voltage difference across diode D1

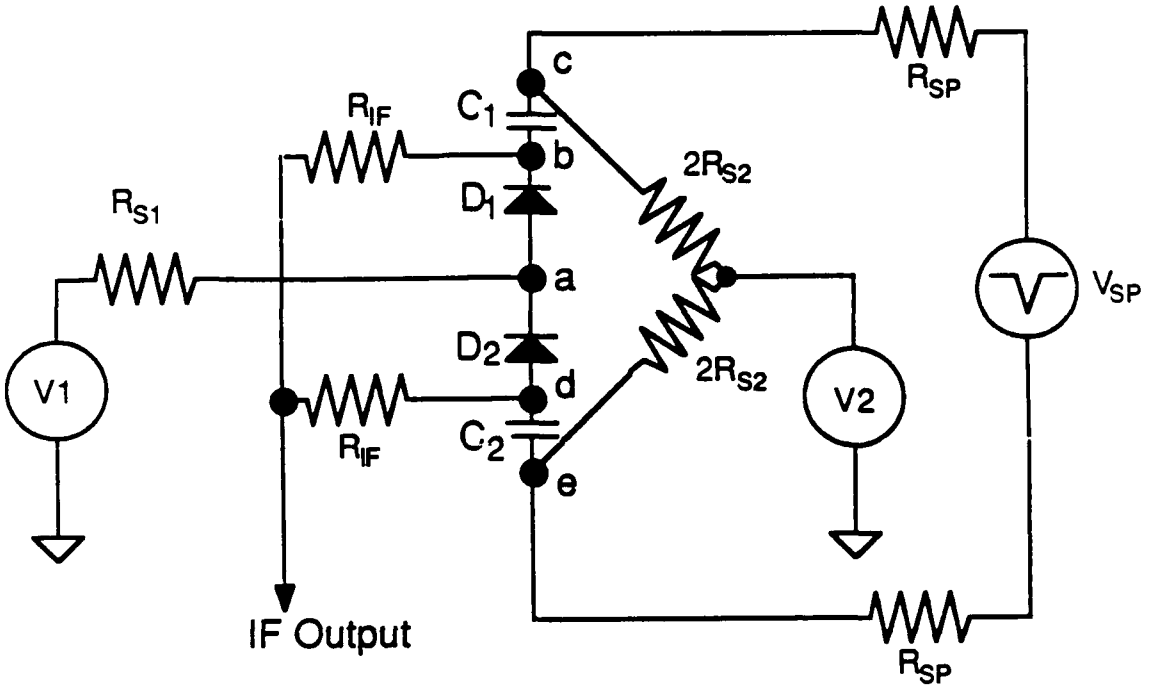

Figure 4.2: Diagram illustrating how a floating voltage can be sampled. The two sources must have constant relative phase.

equal to zero during the peak of the strobe pulse gives, $V_{c1} = V_1 - V_2 - V_{SP}/2$ and $V_{c2} = V_1 - V_2 + V_{SP}/2$ So the voltage at the IF output which is halfway between these two voltages is $V_{IF} = (V1 - V2)/2$. Thus, the voltage at the IF port will follow the voltage difference $V_1 - V_2$ at the IF frequency. This sampler is called a floating sampler because there is an RF potential on both sides of the sampling diodes whereas in conventional samplers, one side of the diode is always zero rf potential. Care must be taken in designing a floating sampler because the IF output nodes, (b) and (d) are no longer at zero rf potential. To avoid loading these nodes, a sizeable IF resistor with substantial inductance at the lowest rf frequency should be used when connecting nodes (b) and (d) to the IF output port. Resistors may be placed in series with the IF output without significant signal degradation because the output

impedance of the samplers at the IF frequency is typically on the order of $20k\Omega$ (see Fig. 3.5).

Finally, the floating sampler is connected to a modified Wheatstone bridge in Fig. 4.3. The left side of the Wheatstone bridge has been split into parallel arms

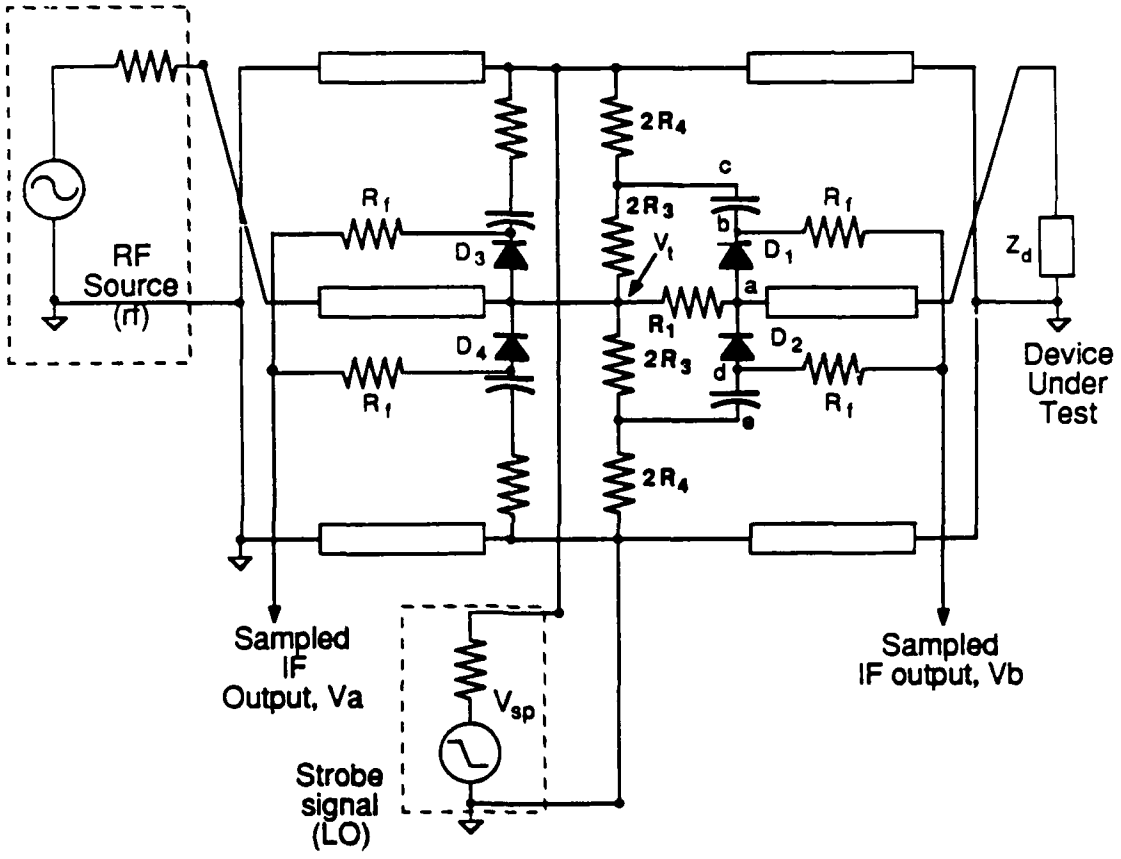

Figure 4.3: Schematic diagram of directional bridge using a floating sampler instead of a balun. The bridge is 'unfolded' to provide a means of strobing the sampling diodes

to provide a means of turning on the sampling diodes (this is the same idea as in splitting the source resistor R_{s2} in Fig. 4.2). The two arms are a mirror image across the horizontal so the rf source which excites them equally will see them in parallel and the rf potential at node (c) will be equal to that at (e). However, the strobe generator, which is applied across the split in the rf ground plane in Fig. 4.3, sees the resistors and the diodes in series. Thus, as described in the previous paragraph,

the IF output of the floating sampler will track the voltage difference from node (a) to node (c) at the IF frequency. So the circuit now performs the function of both the directional device and the sampler B of Fig. 1.2.

Above, it was mentioned that it is desirable to have all resistors in Fig. 4.1a equal to 50Ω. However, when the bridge is unfolded to as discussed above, some of the resistor values must be doubled. Since 100Ω resistors are quite large when fabricated with N^+ material as discussed in Chapter 2, a compromise design is necessary. Removing R_b from the circuit and adjusting the remaining resistors to achieve test-port input-match and balance at $Z_d = R_0$, the reference impedance, yields a set of resistor values all under 100Ω. The voltage at the bridge output is now,

$$V_b = V_t\left(\frac{R_3}{R_4 + R_3}\right)\left(\frac{Z_d - R_0}{Z_d + R_1}\right) \tag{4.3}$$

which is not proportional to the device reflection coefficient Γ_d unless $Z_d \approx R_0$, because $R_1 \neq R_0$. So, to obtain Γ_d based on the measurement of V_b in Eq. (4.3), it is necessary to use a linear fractional transformation (LFT) [4.7] (also called the bilinear or Möbius transformation [4.8]), which has the form $f(z) = \frac{a+bz}{c+dz}$ where z is a complex variable. This is the general form of the transformation used to remove errors in two-port vector network analyzers due to source mismatch, cross-talk between ports, directivity, and transmission loss [4.5]. So, when the test-set is measuring the Γ_d of the device under test, it is as if the usual systematic errors listed above are performing a LFT on the actual value of Γ_d and the transfer function of Eq. (4.3) is performing a LFT on this data. Since the LFT of an LFT is an LFT, and since the LFT is a one-to-one transformation, the same calibration procedure that is used to remove the usual systematic errors will simultaneously compensate for R_1 not being equal to R_0. It can also be shown that having $R_1 \neq R_0$ does not increase the sensitivity of the calibrated data to changes in the absolute value of R_1. From this point of view, the difference between the transfer functions of Eqs. (4.3) and (4.2) is quite superficial.

To provide match at the test port,

$$R_0 = R_1 + \frac{R_s(R_3 + R_4)}{R_s + R_3 + R_4} \tag{4.4}$$

must be satisfied. When Eqs. (4.4) and (4.1) are both satisfied,

$$R_4 = \frac{R_0^2(R_0 - R_1)}{R_1(R_0 + R_1)}$$

For the monolithic directional sampler, the following values were used:

$$R_1 = 25\Omega, R_3 = 16.7\Omega, R_4 = 33.3\Omega, R_s = 50\Omega$$

Even though R_3 and R_4 must be doubled, as in Fig. 4.3, the entire set of values is less than 100Ω and easily implemented with N^+ material.

The second sampler, sampler A of Fig. 1.2, can be readily added to the circuit by simply connecting a sampler of the non-floating variety on the left side of Fig. 4.3. This sampler is driven from the same source as the floating sampler, so no additional strobe generator is needed. Since this sampler directly measures, V_t, the Γ_d dependance of V_t is not important as it will be divided out. The completed circuit now replaces both samplers as well as the directional device of Fig. 1.2. By using coplanar waveguide (CPW) for the transmission line sections of Fig. 4.3, the entire circuit can be fabricated in a monolithic integrated circuit.

4.3 Monolithic directional sampler

4.3.1 Design and layout

A plan view of the directional sampler is shown in Fig. 4.4. The directional sampler was fabricated on a semi-insulating GaAs substrate using the process described in Chapter 2. The strobe pulse is generated by a hyperabrupt-doped NLTL [4.9] on a separate chip. This pulse is applied across the narrow CPW grounds from the bottom port. The rf excitation is provided to the port on the left of Fig. 4.4, and the right port is connected to the device under test. The CPW grounds are shorted together by airbridges 250μm from the center to provide a 5 ps round-trip time for the applied sampling pulse which has a transition time of approximately 5 ps. When the strobe pulse is applied, V_t and V_b are simultaneously sampled. The down converted signals are filtered by 100Ω resistors and delivered to bond pads on the left and right sides of the chip.

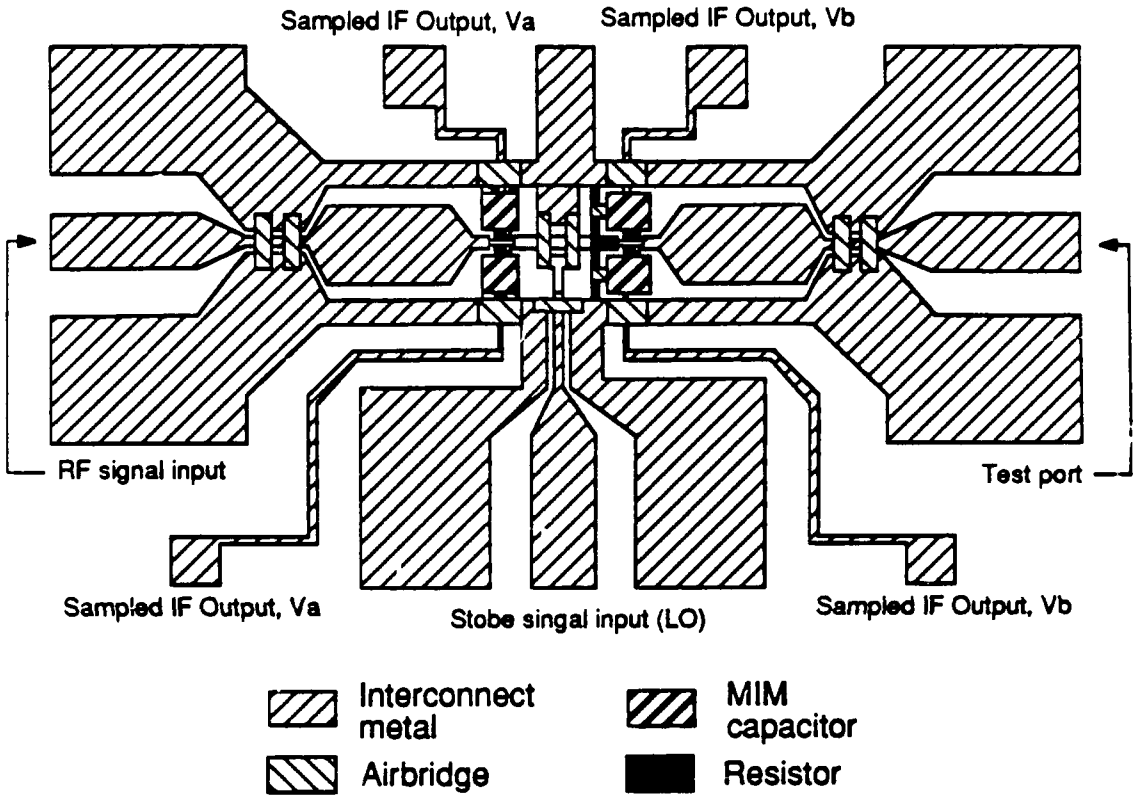

Figure 4.4: Layout of the directional sampler.

The resistors of the directional bridge were 5 μm wide. The small size was necessary to fit all five resistors in the small space between the two rf grounds. Because of the variations in contact resistance described in Chapter 2, these resistors have a tolerance of 22%. Differentiating Eq. 4.3 gives the sensitivity of the output voltage of the bridge for $Z_d = R_0$ normalized to the output voltage for $Z_d \rightarrow \infty$,

$$\frac{\partial V_b(Z_d = R_0)}{V_b(Z_d \rightarrow \infty)} = \frac{-2}{3}\left\{\frac{\partial R_1}{R_1} - \frac{\partial R_3}{R_3} + \frac{\partial R_4}{R_4}\right\} \tag{4.5}$$

The measured values for a typical die were $R_1 = 20\Omega$, $R_3 = 18\Omega$, $R_4 = 30\Omega$. Using

these values and the design values in Eq. (4.5) yields a predicted output voltage for a matched load normalized to the open circuit voltage of 0.24 or 12.4 dB. This number is the effective directivity of the bridge.

4.3.2 Results

Because the directional sampler, like any sampler, has a relatively high impedance IF output (see Fig. 3.5), it is difficult to perform on-wafer testing of the monolithic directional sampler circuits without cross-talk between the IF outputs or excessive capacitive loading. So, the circuits were diced and assembled with a NLTL strobe pulse generator in a 60 GHz package using Wiltron V-connectors[1] on the rf and test ports. The IF output bond pads were connected to the low-frequency output pins on the package with ~1 cm bond wires to help filter out any rf. An rf signal between 2 and 60 GHz was applied to the rf port while the NLTL drive (LO) was maintained between 2 and 6 GHz, so that the proper harmonic mixes the rf signal and the floating bridge voltage down to the 90 MHz IF frequency (see Fig. 4.5). Two external mixers were then used to convert the IF to the 20 MHz used by the Hewlett-Packard 8510B network analyzer. The 'first' IF was chosen to be 90 MHz so that the Wiltron 90 MHz buffer amplifier could be used. The 8510B was used as the vector receiver because it was readily available and easily adapted to drive the rf and LO signal generators at the proper frequencies.

With the directional sampler configured as described above, it can be used as a one-port S-parameter test set for the 8510B. Two types of measurements were made in this mode. First, the uncalibrated reflection coefficient (simply the ratio of the two IF vector voltages) was measured for an open, load and a short. The difference in magnitude between the uncalibrated reflection coefficient of the open and that of the load is a measure of the directivity. This is an imperfect directivity measurement since imperfections in the load or losses in the open will degrade the observed difference. However, this measurement puts a lower bound on the directivity. The directional sampler required large LO power (~ 30 dBm) drive to

[1] V-connector is a trademark of Wiltron Company

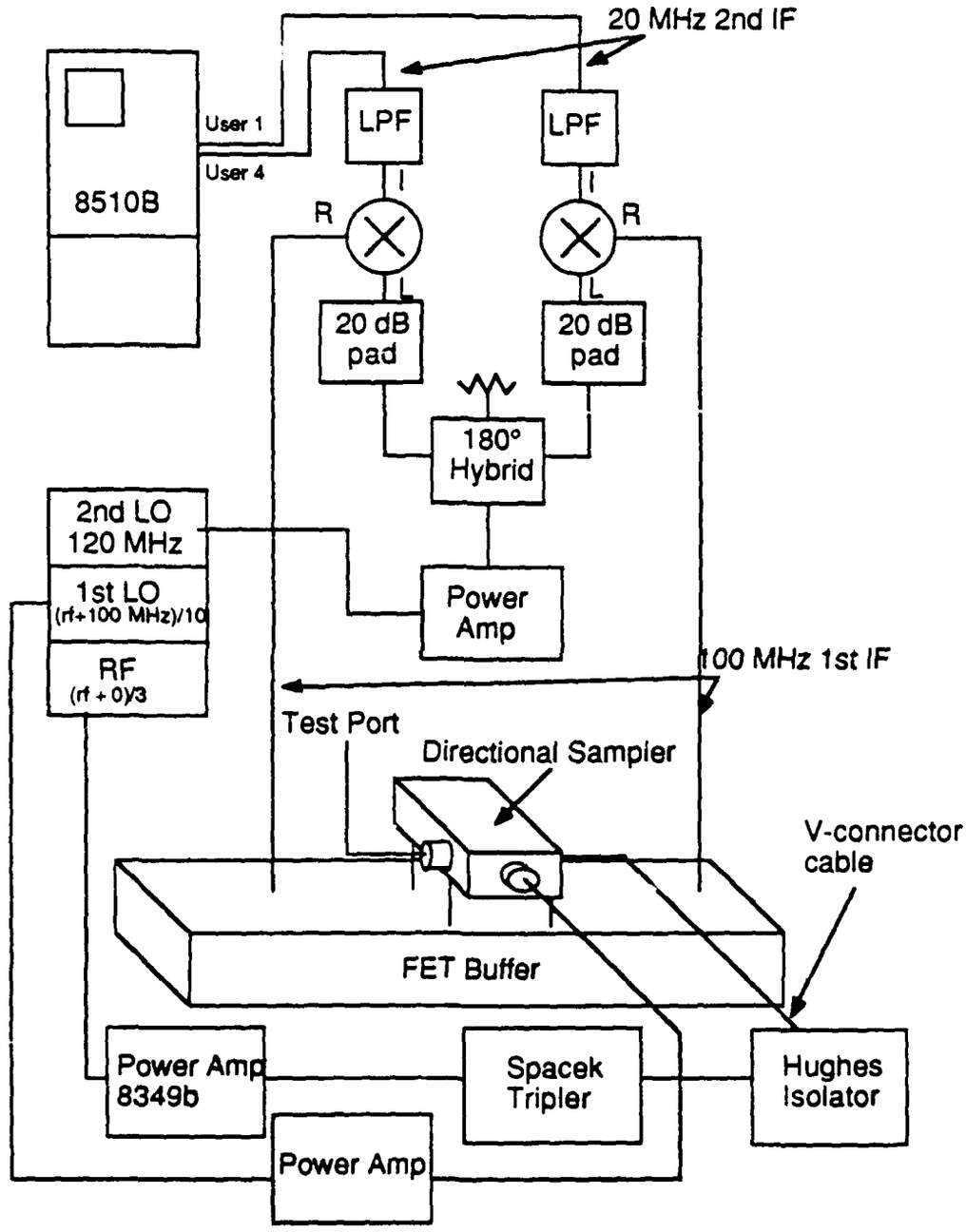

Figure 4.5: Directional sampler S-parameter test set-up. The 8510B in external mixer mode, controls the two synthesizers to produce a signal at the 90 MHz first-IF.

the NLTL for optimum performance. This power was available between 2-4 GHz so measurements were made using this LO range and an rf frequency from 2 to 4 GHz, 4 to 8 GHz, 8 to 16 GHz, 12 to 24 GHz, 20 to 40 GHz (using a frequency doubler), and 40 to 60 GHz (using a frequency tripler). The directivity over the entire 2 to 60 GHz range was better than 10 dB. A typical result is shown in Fig. 4.6. Next,

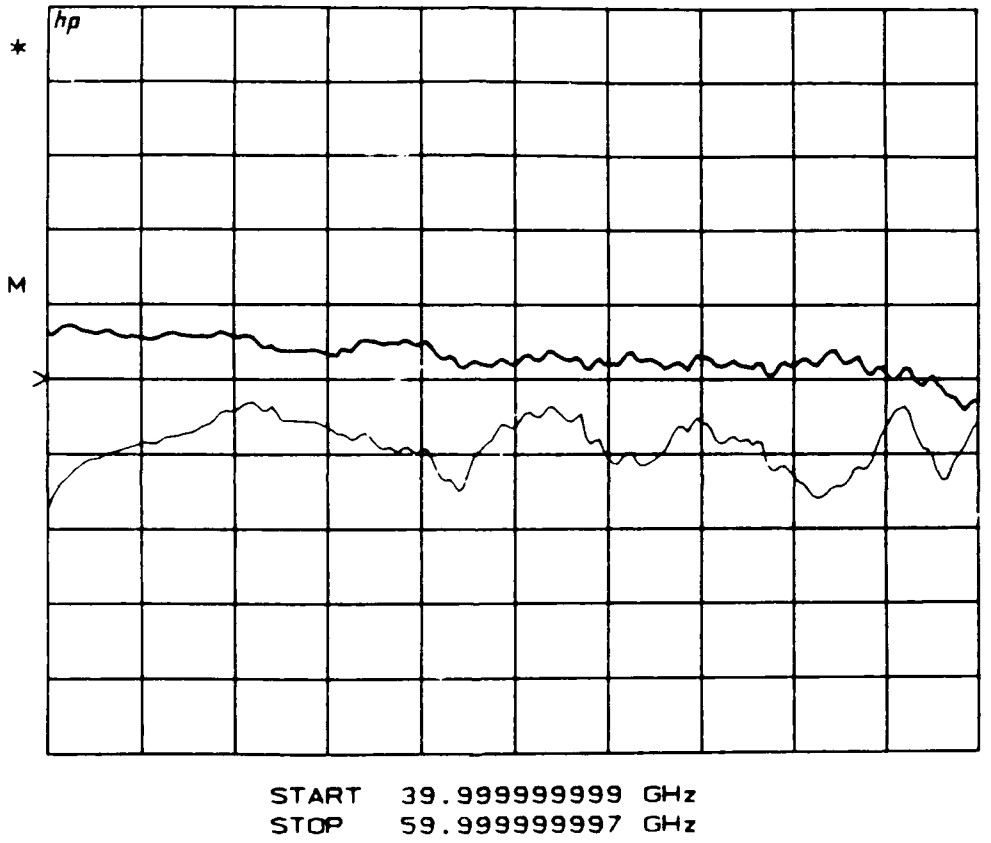

Figure 4.6: Uncalibrated S-parameter measurement with the directional sampler from 40 to 60 GHz. The heavy trace is the magnitude of the reflection from an open V-connector. The lighter trace is that of a load with a 2.4 mm connector.

a calibrated S-parameter measurement was performed. The standard "open-short-load" calibration procedure was used over a frequency range where connector losses were low and therefore the effective directivity was as high as possible. Figure 4.7 shows a typical calibration over the 8-16 GHz band. The calibration was limited to a single band at a time since the 8510B software can not skip LO harmonic numbers.

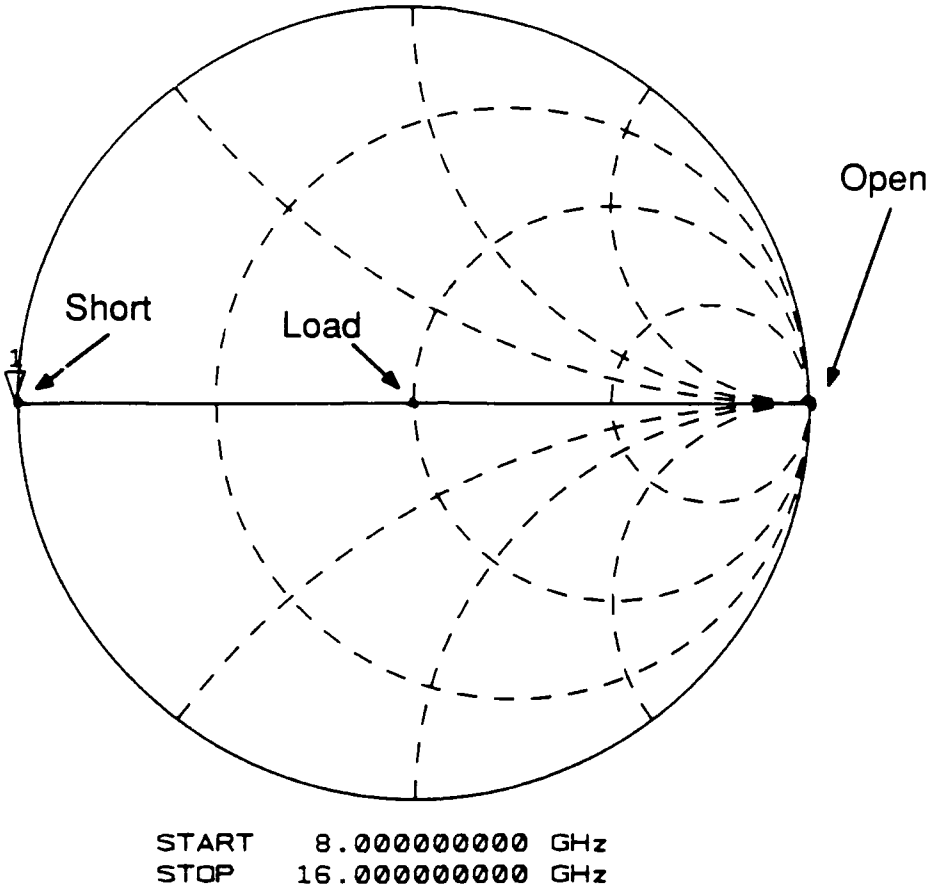

Figure 4.7: Open, short, and load measured by the directional sampler after calibration.

While 10 dB directivity to 60 GHz is no better than the best available coaxial directional coupler, the potential exists for much greater directivity and bandwidth. The measured 10 dB directivity is quite close to the predicted 12 dB directivity based solely on resistor values. If thin-film resistors trimmed within 10% of design value were added to the process, the directivity could be improved to 14 dB. If the sign of the resistor error was the same for all resistors (that is, if they were all high or all low) the directivity could be improved again to 23 dB. This directivity is independent of frequency since it is determined by the values of low-parasitic resistors. Therefore, using the techniques of Chapter 3, fabricating a 100 GHz, 20 dB directivity directional sampler should be a straightforward task, once a slightly

better resistor process is developed.

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Chapter 5

Distributed frequency multiplication

5.1 Introduction

Efficient frequency multipliers are important in a variety of systems. At millimeter-wave frequencies frequency multiplication is often the only practical way to achieve a phase-locked source of radiation [5.1]. Archer [5.2] has achieved 7.5 dB doubler conversion loss over a bandwidth of 90 to 124 GHz with a whisker-contacted varactor diode in a waveguide mount. While this result is impressive, a millimeter-wave doubler exploiting the distributed nonlinear interaction on a monolithic nonlinear transmission line (NLTL) [5.3] offers a much more compact, less expensive, and possibly more efficient method of harmonic generation. As a proof of this principle, Wedding and Jäger [5.4] have demonstrated 90% conversion efficiency on a macroscopic NLTL at radio-frequencies, through doubling from a forward to a *backward* wave in the upper passband of a periodic line. However, the tunability of this structure is not discussed. In this chapter, theory and experimental results of second-harmonic-generation (SHG) through doubling up from a forward wave to a *forward* wave in the upper passband of a modified NLTL is presented. This structure offers a broad electrical tuning range with reasonable impedance matching at both fundamental and second harmonic frequencies.

5.2 The diatomic lattice

To accomplish high efficiency SHG on a distributed network with large nonlinearity, it is necessary to prevent shock-wave formation, provide phase matching between the input and second-harmonic frequencies, and suppress higher order harmonics. One structure that accomplishes these goals is the electrical analogue of the diatomic lattice [5.5] shown in Fig. 5.1. The dispersion relation of the diatomic lattice is given

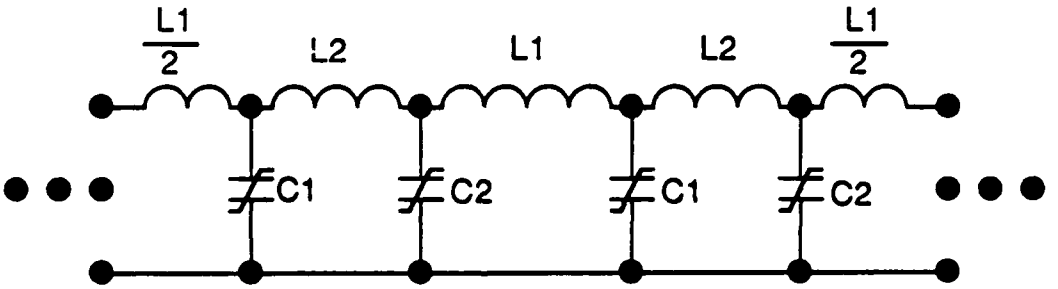

Figure 5.1: Electrical analog of the diatomic lattice. Inductance, L, replaces the atomic mass and capacitance C, replaces the spring constant.

by

$$\omega^2 = \frac{1}{2}\left(\frac{1}{L_1}+\frac{1}{L_2}\right)\left(\frac{1}{C_1}+\frac{1}{C_2}\right) \pm \sqrt{\frac{1}{4}\left(\frac{1}{L_1}+\frac{1}{L_2}\right)^2\left(\frac{1}{C_1}+\frac{1}{C_2}\right)^2 - \frac{4sin^2(k/2)}{L_1L_2C_1C_2}} \quad (5.1)$$

where L_1 and L_2 are shown in Fig. 5.1, C_1 and C_2 are the shunt capacitances of the varactor diodes, and k is the propagation constant in units of radians/section. The + root defines the upper branch and the − root defines the lower branch of the dispersion diagram in Fig. 5.2. From Fig. 5.2 it is evident that if the band gap is made sufficiently small, phase matched doubling from a forward wave on the lower branch to a backward wave on the upper branch is possible, as demonstrated by

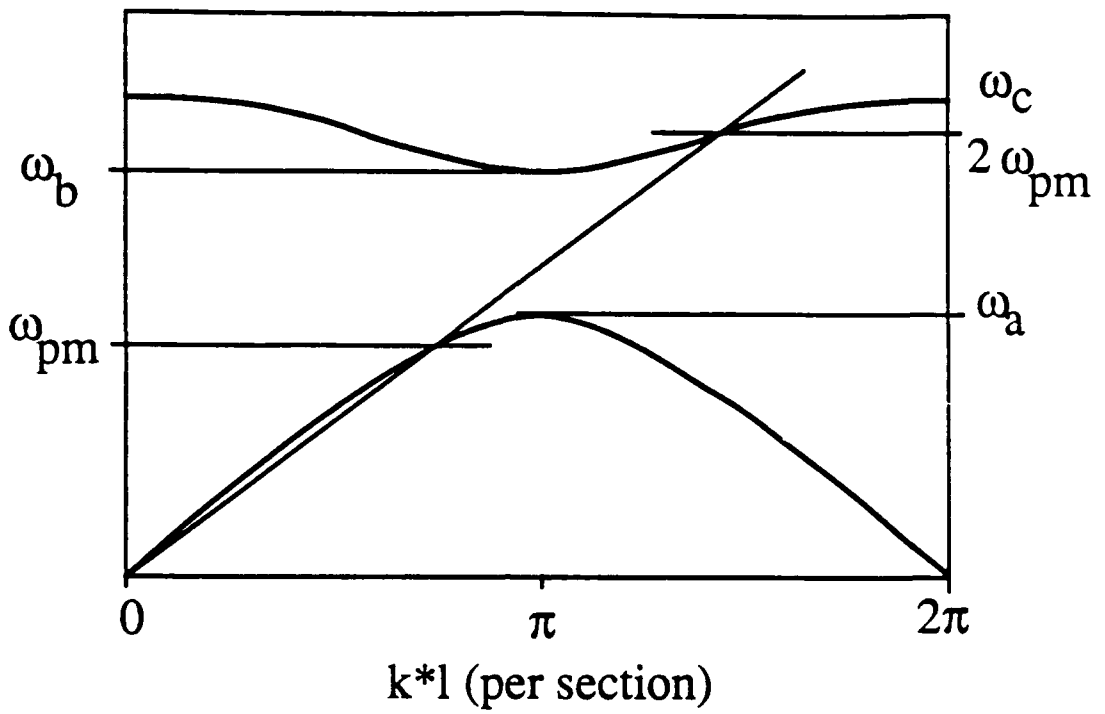

Figure 5.2: Dispersion relation of the diatomic lattice, showing the phase-matching condition and the band edges. At a fundamental frequency ω_{pm}, the phase matching condition is satisfied. The first band edge is $\omega_a = \sqrt{\frac{2}{L_1 C}}$, the beginning of the second band is $\omega_b = \sqrt{\frac{2}{L_2 C}}$, and the high-frequency cut-off is $\omega_c = \sqrt{\frac{2}{C}(\frac{1}{L_1} + \frac{1}{L_2})}$.

Wedding and Jäger. However, if an attempt is made to tune the operating frequency by adjusting C_1 or C_2, the band-gap will widen and possibly prevent propagation of the second harmonic. To avoid this problem, the choice $C_1 = C_2 = C$ was made so that the shape of the dispersion relation is determined by the lithographically defined ratio L_1/L_2. Also, the doubler is designed to work with a fundamental forward wave and a second harmonic forward wave (Fig. 5.2). The phase matching condition for this case is

$$\omega_{pm} = \sqrt{\frac{2}{L_1 C}} \sqrt{1 + \frac{L_1}{L_2} - \sqrt{\frac{3L_1}{L_2}}} \tag{5.2}$$

This shows that phase matching can be accomplished over the entire tuning range of the capacitor C. Choosing the ratio L_1/L_2 equal to 2.421, places the second

harmonic in the middle of its pass-band for all values of C, when the fundamental is driven at the tunable frequency ω_{pm}.

Finally, the characteristic impedance of the structure is given by

$$Z_{B1,2} = \sqrt{\left(\frac{L_1 + L_2 - \omega_{1,2}^2 L_1 L_2 C/2}{2C}\right)\left(\frac{1 - \omega_{1,2}^2 L_1 C/2}{1 - \omega_{1,2}^2 L_2 C/2}\right)} \tag{5.3}$$

where $Z_{B1,2}$ is the characteristic impedance at the fundamental ω_1 and the second harmonic ω_2, respectively. It is not possible to simultaneously impedance match and phase match at both frequencies, so an impedance match is chosen only at the second harmonic. Combining the requirements of centering the second harmonic in its band, phase matching, and impedance match at the second harmonic yields

$$C = \frac{0.2489}{\omega_1}, L_1 = \frac{58.32}{\omega_1}, L_2 = \frac{37.48}{\omega_1}$$

5.3 Nonlinear analysis

If C is allowed to be nonlinear, and curve-fit a second order polynomial to the measured C-V relation in the region of interest,

$$C(V - V_0) = C^{(0)} + C^{(1)}(V - V_0) + C^{(2)}(V - V_0)^2$$

$C(V - V_0)$ can be substituted into the circuit equations of the structure to obtain the coupled mode equations [5.6]

$$\frac{da_{1+}}{dz} = -(\alpha_1 + jk(\omega))a_{1+} - jK_1 a_{2+} a_{1+}^* \tag{5.4}$$

$$\frac{da_{2+}}{dz} = -(\alpha_2 + jk(2\omega))a_{2+} - jK_2 a_{1+}^2 \tag{5.5}$$

$$K_1 = \sqrt{2Z_{B2}} Z_{B1} \omega_1 C^{(1)}$$

$$K_2 = \sqrt{2Z_{B1}} Z_{B2} \omega_1 C^{(1)}$$

Here, $a_{1,2+}$ are the forward traveling waves at the fundamental and second harmonic, respectively. They are related to the instantaneous voltage by the equation

$$V = \sqrt{2Z_{B1}}(a_{1+}e^{j\omega t} + a_{1+}^* e^{-j\omega t}) + \sqrt{2Z_{B2}}(a_{2+}e^{j2\omega t} + a_{2+}^* e^{-j2\omega t})$$

Here, $\alpha_{1,2}$ are the attenuation constants in Np/section at the fundamental and second harmonic respectively.

The coupled mode Eqs. (5.4), (5.5) are derived by first assuming a uniformly distributed transmission line with nonlinear capacitance, and then replacing $\omega_1 Z_{B1} C^{(0)}$ with $k(\omega_1)$ and $2\omega Z_{B2} C^{(0)}$ with $k(\omega_2)$. This allows the correct dispersion relation to be used, while separating the problem of determining the dispersion from the nonlinear problem. Terms involving $C^{(1)}$ yield the usual equations for SHG, while terms with $C^{(2)}$ add the effect of the power dependant phase-velocity, which can adversely effect phase-matching.

In the present case, losses turned out to be more important than pump depletion due to conversion or $C^{(2)}$ effects, so an analysis similar to the analysis of Champlin et. al. [5.7] can be used. This yields the solution

$$a_{2+} = \left(\frac{K_2 a_{10}^2}{\alpha_2 - 2\alpha_1}\right)\left(e^{-2\alpha_1 z} - e^{-\alpha_2 z}\right) \tag{5.6}$$

which has a maximum at

$$z = \frac{1}{2\alpha_1 + \alpha_2} \ln\left(\frac{2\alpha_1}{\alpha_2}\right) \tag{5.7}$$

where the conversion efficiency will be

$$\eta_{max} = \left[\frac{K_2 a_{10}}{\alpha_2}\left(\frac{\alpha_2}{2\alpha_1}\right)^{\frac{1}{1-\frac{\alpha_2}{2\alpha_1}}}\right]^2 \tag{5.8}$$

5.4 Losses on the distributed doubler

Equation (5.8) shows that the conversion efficiency is critically dependent on the attenuation at the fundamental and second harmonic. Resistance of the interconnecting transmission lines, diode series resistance, and radiation all contribute to the attenuation of the doubler line. The attenuation coefficients due to conductor and dielectric loss on a TEM transmission line are

$$\alpha_c = \frac{R}{2Z}, \quad \alpha_d = \frac{G_d Z}{2} \tag{5.9}$$

where R is the effective resistance per unit length of the transmission line, Z is the characteristic impedance of the line, and G_d is the dielectric conductance per unit

length. The inductors L_1 and L_2 will be implemented with short, high-impedance sections of coplanar waveguide (CPW) and the capacitors with reverse biased Schottky diodes, as with the NLTL. Conductor loss on CPW is given by [5.8]

$$\begin{aligned} \alpha_c^{CPW} &= 5.62 \times 10^{-5} R_s \epsilon_{re} Z_{0cp} \frac{P'}{\pi W}(1 + \frac{S}{W}) \\ &\times \left\{ \frac{\frac{1.25}{\pi} \ln \frac{4\pi S}{t} + 1 + \frac{1.25t}{\pi S}}{\left[2 + \frac{S}{W} - \frac{1.25t}{\pi W}(1 + \ln \frac{4\pi S}{t})\right]^2} \right\} \end{aligned} \tag{5.10}$$

$$\epsilon_{re} \approx \frac{\epsilon_d + 1}{2} \tag{5.11}$$

$$R_s = \sqrt{\frac{\omega \mu \rho}{2}} = 9.81 \times 10^{-3} \sqrt{\frac{f}{1\ \text{GHz}}} \tag{5.12}$$

$$P' \approx \frac{\pi^2}{2\mathbf{k} \ln^2 \frac{4}{\mathbf{k}}} \text{ for } \mathbf{k} < 0.1 \tag{5.13}$$

$$\mathbf{k} = \frac{S}{S + 2W} \tag{5.14}$$

where α_c is the loss in Np/unit length on a coplanar waveguide with center conductor width S, center conductor to ground spacing W, characteristic impedance Z_{0cp}, surface resistance R_s, and metal thickness t patterned on a substrate with a relative dielectric constant of ϵ_d. Equating Eq. (5.10) with the conductor loss expression in Eq. (5.9) yields an effective series resistance for the unloaded transmission line, $R_{CPW} = 2Z_{0cp}\alpha_c^{CPW}$. When the capacitances of the shunt connected Schottky diodes are connected to the CPW, the characteristic impedance will be changed to that given by Eq. (5.3) but the physical resistance R_{CPW} will not change. The attenuation coefficient due to conductor losses of the diode loaded line is therefore

$$\alpha_c = \frac{Z_{0cp}}{Z_B} \alpha_c^{CPW} \tag{5.15}$$

Losses due to shunt conductance are dominated by the Schottky diode losses. The diode model is simply a series resistance R_d and a large signal junction capacitance C_{l_s}. The series R_d, C_{l_s} network can be converted into a parallel G_d, C_{l_s} network where the shunt conductance G_d is given by

$$G_d = \omega^2 C_{l_s}^2 R_d \tag{5.16}$$

Combining Eq. (5.16) with the expression for α_d in Eq. (5.9) yields the attenuation in Np/diode due to diode series resistance. Since there are two diodes per doubler section, the attenuation per section is

$$\alpha_d = \omega^2 C_{js}^2 R_d Z_B \tag{5.17}$$

Radiation losses are much more difficult to quantify. However, a qualitative analysis can reveal at least the order of magnitude. Figure 5.3 shows how the currents of the doubler line can be represented by an array of dipoles. The dipole

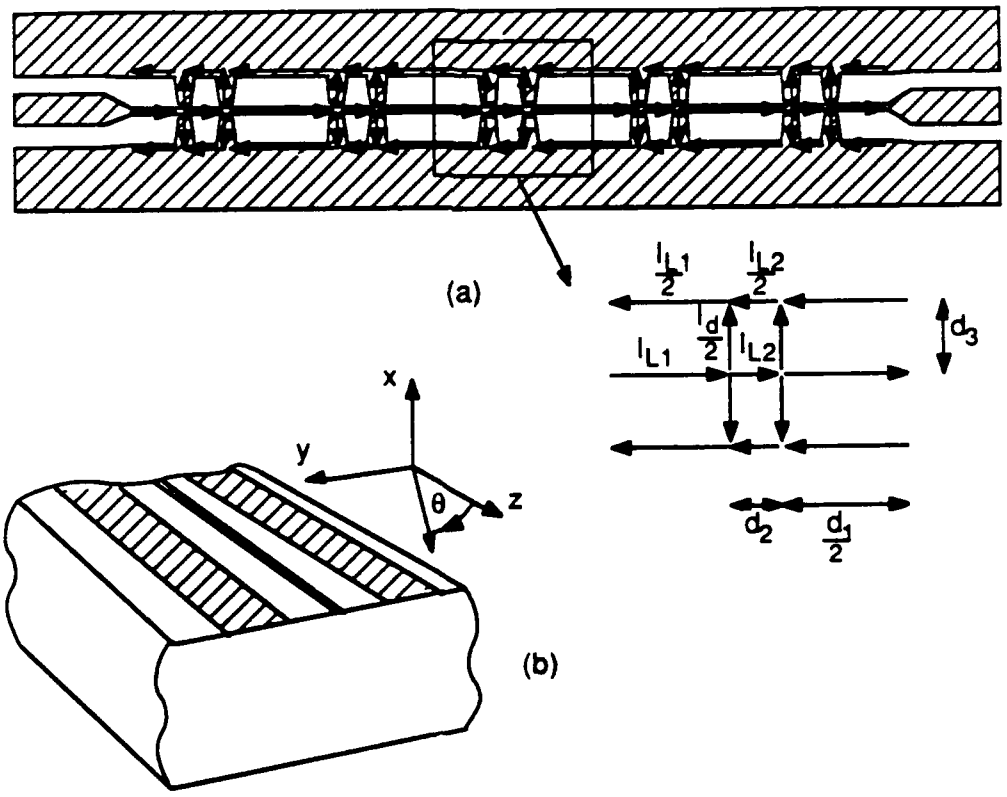

Figure 5.3: Radiation sources on the distributed doubler. The dipole representation of a section is shown in the inset. The CPW geometry and coordinate system is also shown (b).

representation of a section shown in the inset is repeated with a spacing $d_1 + d_2$. If

the far field, or Fraunhofer diffraction pattern of the section is $f(\theta, \phi)$, then, using the principle of pattern multiplication, the total radiation pattern of the doubler line is

$$f_T = f(\theta, \phi) \frac{\sinh \frac{M\gamma}{2}}{\sinh \frac{\gamma}{2}} \tag{5.18}$$

where M is the total number of sections and

$$\gamma = j \left\{ \frac{2\pi(d_1 + d_2)}{\lambda} \cos\theta - k(\omega) \right\} - \alpha \tag{5.19}$$

where λ is the wavelength in the substrate material, $k(\omega)$ is the phase shift per section given by Eq. (5.1), and α is the total loss per section. The radiated field is maximized when

$$\frac{2\pi(d_1 + d_2)}{\lambda} \cos\theta - k(\omega) = 2n\pi; \text{ n } = 0, \pm 1, \pm 2, \pm \ldots \tag{5.20}$$

This is satisfied when

$$\cos\theta = \frac{(2n\pi + k(\omega))\lambda}{2\pi(d_1 + d_2)} \tag{5.21}$$

When $n = 0$, Eq. (5.21) reduces to the usual condition for Cherenkov radiation. However, because this is a periodic and not a uniform transmission line, the additional solutions with $n \neq 0$ exist. These extra solutions have no effect on the lower branch of the dispersion relation, but allow significant portions of the upper branch to radiate. Therefore, to minimize loss due to radiation in the upper branch, the section pattern amplitude $f(\theta, \phi)$ must be minimized by making d_3 as small as possible.

5.5 Results

A monolithic frequency doubler using $L_1 = 186pH$, $L_2 = 77pH$, and $C = 79fF$ was designed. The layout and dimensions are shown in Fig. 5.4. The inductances of the CPW sections are $L_{1,2} = d_{1,2} Z_{0cp}/v$ where v is the phase velocity on the unloaded CPW. The impedance of the CPW is 90Ω so the L_1 section is 219 μm long and the L_2 section is 83 μm long. The capacitance of the L_1 line section is 22 fF and is 8.2 fF for the L_2 section. Consistent with previous NLTL designs

using 90Ω line sections, the center conductor width was chosen to be 10 μm , with a 60 μm spacing to ground. The stray capacitance in parallel with the Schottky diode is estimated to be 4.4 fF, using a CPW model. The total line capacitance per diode is $11 + 4.1 + 4.4 = 19.5fF$. The balance of the 79 fF is provided by the Schottky diode with 1.5 volt reverse bias, so the zero bias junction capacitance is $C_{j0} = 100fF$. The doublers were placed on the same mask as the generation III samplers so the N^- layer was 0.3 μm thick and uniformly doped at 1.2×10^{17}. The diode area for the 100 fF C_{j0} on this material is $4x20$ μm . The Schottky diodes and interconnecting CPW were formed according to the process described in Chapter 2.

Based on Eqs. (5.15) and (5.17) the total attenuation excluding radiation loss is expected to be $\alpha_c + \alpha_d = 0.056 + 0.022 = 0.078$ Np/section at 50 GHz and $0.079 + 0.088 = 0.17$ at 100 GHz. A curve fit to the measured C-V relation of the doubler line gives $C^{(1)} = 13.6$ fF/V. For a 20 dBm input, $K_2 a_{10} = 0.45$ radians/section. The predicted conversion based on these values is greater than 100%, invalidating the assumption that the fundamental is not depleted by conversion. However, the actual losses were significantly greater and K_2 was smaller than expected.

The doublers were tested using direct-electrooptic sampling (described in Chapter 1). Preliminary measurements used the 0 dBm output of a frequency tripler at 48.8 GHz. A more detailed study was performed using the multiplier to injection-lock a $\sim$ 20 dBm, 50 or 55 GHz oscillator to a harmonic of the probe laser pulse repetition rate plus 600 kHz. The 50 or 55 GHz signal was down-converted to 600 kHz by electrooptic mixing while the second harmonic was found at 1.2 MHz. The amplitude response of the electrooptic sampler was calibrated using a lower frequency signal at the same offset. The experimental set-up is shown in Fig. 5.5.

Two doubler designs were evaluated. The first design, having 5 sections, was a straight CPW transmission line with 10 diodes. The second design, having 17 sections, was a 34-diode CPW structure which included four 90 degree bends in order to reduce the circuit size. Preliminary measurements on the 17-section doubler with 0 dBm of input power at 48.8 GHz and 1V reverse bias on the line gave results in reasonable agreement theory up to the first bend. The loss at the fundamental was

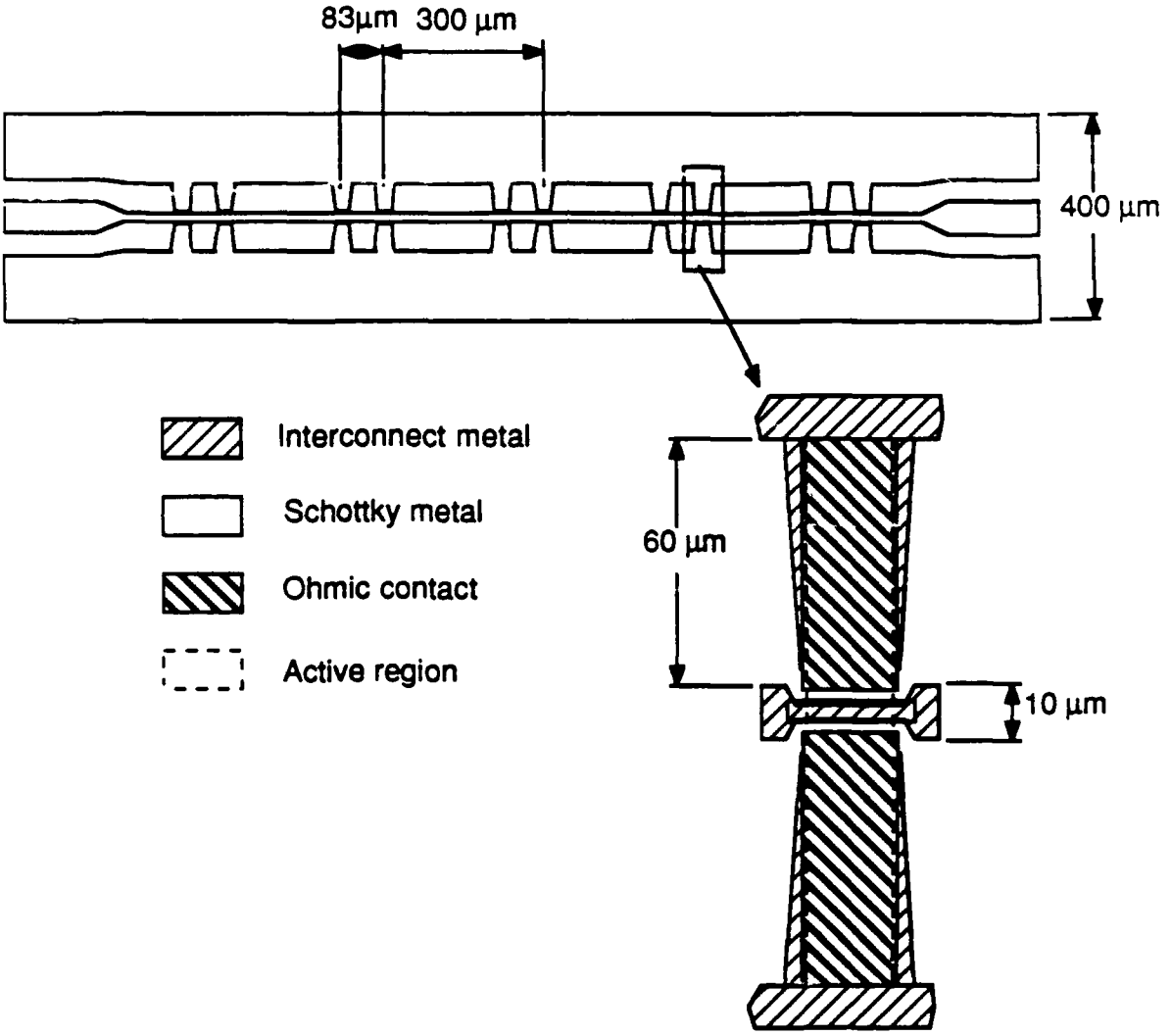

Figure 5.4: Layout of the distributed frequency doubler.

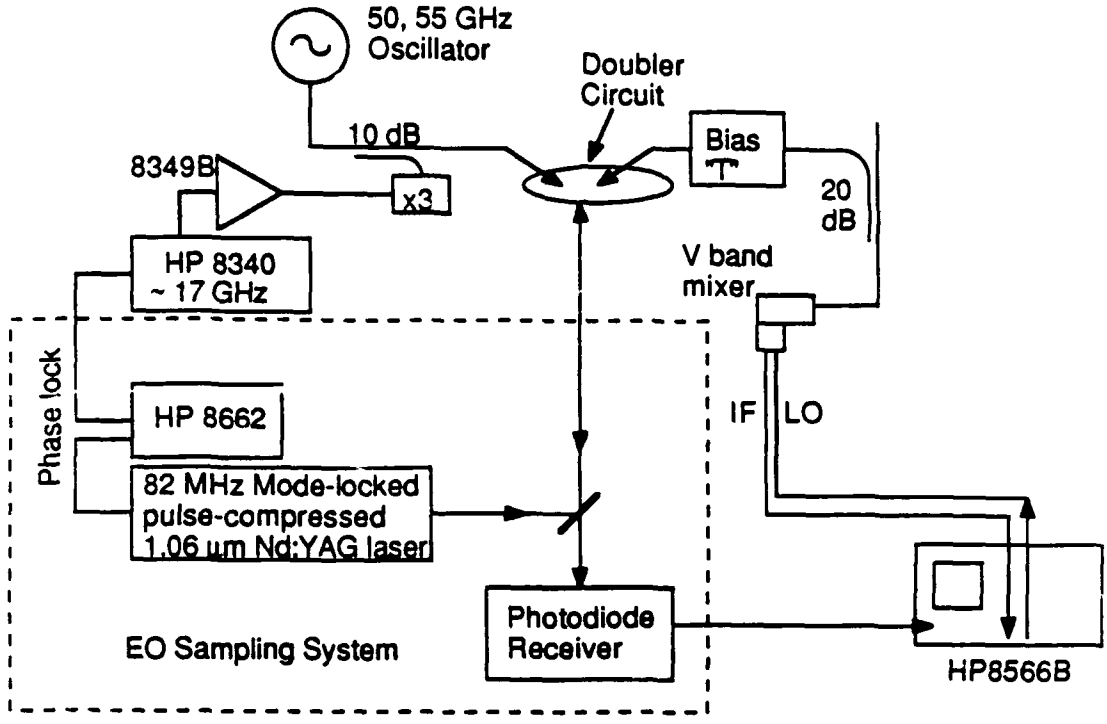

Figure 5.5: Experimental set-up for testing the monolithic doublers.

$\approx$ 0.08 Np/section and the minimum conversion loss was 22 dB compared with the theoretical value of 20 dB from Eq. (5.8). The second harmonic amplitude peaked near the end of the first 5 sections, whereas Eq. (5.7) predicts a peak at the sixth section using the theoretical losses.

Although the preliminary measurements showed that the doubler was working in accordance with theory, 1% conversion efficiency does not compare well with other available frequency multipliers. Jim Crowley of Varian III-V device center provided two high-power oscillators for the investigation of higher conversion efficiency. Figures 5.6 and 5.7 show a comparison of the theoretical and experimentally obtained values for both designs. In the 5-section doubler, maximum powers of 2 and 5 dBm were measured with input powers of 14 and 21 dBm at 50 and 55 GHz respectively. The discrepancy between theory and measurement is mainly due to the standing wave generated by the bad match of the 50 GHz wafer probe at the output of the doubler. The 17-section doubler showed better agreement between theory and mea-

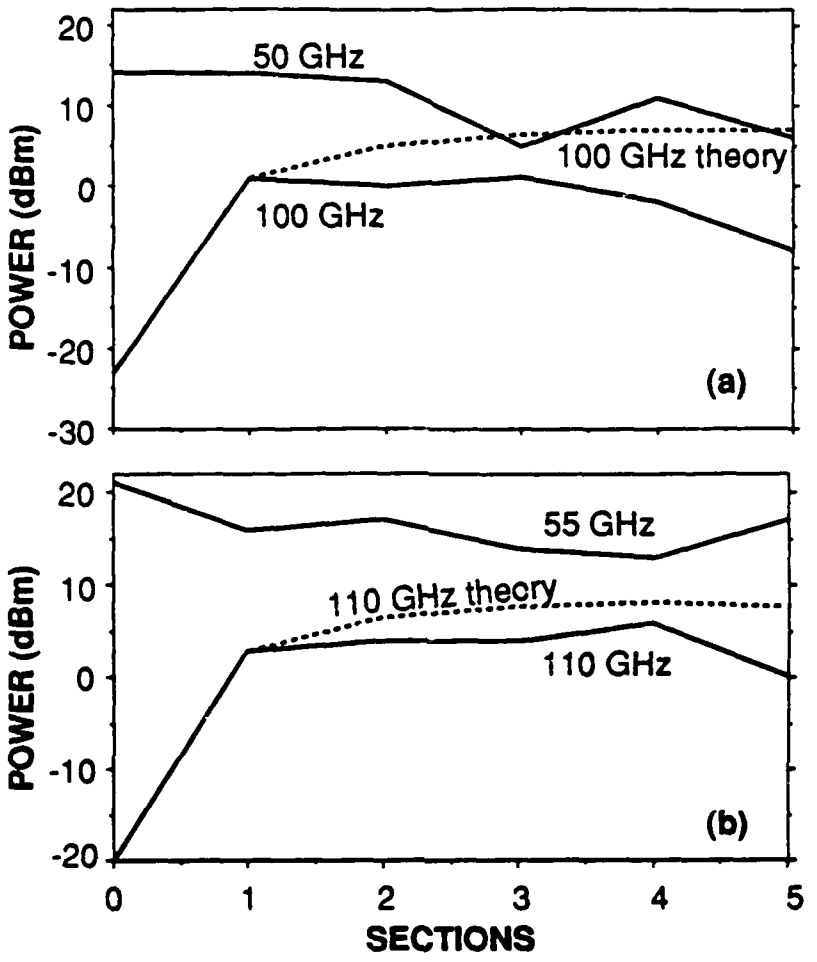

Figure 5.6: Comparison of the theoretical and experimental second harmonic generation for the 5-section doubler. Experimental data for the 50 GHz fundamental and the 100 GHz second harmonic are plotted as a function of position (solid lines) in (a). The theoretical prediction is shown by the dashed curve. The experiment was repeated with a 55 GHz fundamental and 110 GHz second harmonic (b).

surement because the high losses of the circuit minimized the standing wave effect. A maximum power of 10 dBm was measured at 100 GHz at stage 5, but it was reduced by 8 dB at stage 6, after the 90 degree CPW bends. The 110 GHz data was comparable to the 100 GHz measurement. The theoretical data assumes 50, 55, 100 and 110 GHz line losses of 0.11, 0.13, 0.24 and 0.266 Np/section respectively and $K_2 a_{10}$ of 0.14 and 0.08 at 50 and 55 GHz respectively. Although the theory predicts the shape of the curve well enough, the values necessary to achieve this fit are not

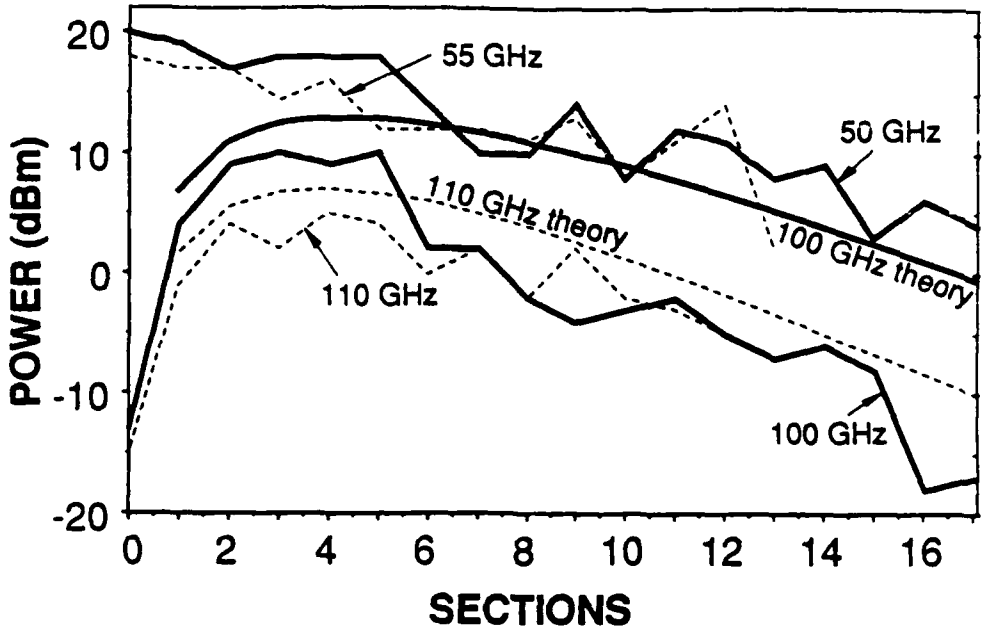

Figure 5.7: Comparison of the theoretical and experimental second harmonic generation at 100 and 110 GHz for the 17-section doubler. Experimental data for the 50 GHz fundamental, the 100 GHz second harmonic, and the predicted 100 GHz values are plotted as a function of position (solid lines). The experiment was repeated with a 55 GHz fundamental and 110 GHz second harmonic (dashed lines).

at all in agreement with those predicted.

5.6 Conclusion

The results of the previous section indicate that phase-matched second harmonic generation has been accomplished to some degree. However, the anomalously low value of K_2 indicates that the doubler was not functioning in accordance with theory in the high-power experiment. One contributor to this problem is the fact the line was designed to operate at a reverse bias of 1.5 V but was driven with a 3V sinusoid. Therefore, when the diodes were properly biased for phase-matching, they were driven into forward conduction by the fundamental. Such power was necessary to achieve significant conversion on the short line that was available. Another factor

could be the power-dependant phase velocity briefly mentioned previously. Further analysis is necessary to investigate the magnitude of this effect. If this is a limiting factor, it can be reduced by designing the doping of the epitaxial layer such that a linear capacitance change with voltage is achieved, thus making $C^{(2)} = 0$.

The loss at 100 GHz could be partially circumvented if spatial power combining is used instead of phase matching guided waves. This technique has been used for second harmonic generation of optical radiation in lithium niobate [5.9]. The fundamental propagates in the waveguiding structure while the second harmonic radiates into the substrate in a semicone with angle θ given in Eq. (5.21). In section 5.4 it was pointed out that, while the structure does radiate, the radiation can be minimized by keeping the transverse dimension small. On the other hand, if the transverse dimension is increased, the structure can radiate with high efficiency. There are several benefits of this approach. First, since the second harmonic is being radiated, the transmission line parameters can be optimized for the fundamental frequency. Second, large, low impedance, low loss CPW sections may be used to connect the Schottky diodes. The characteristic impedance can be raised to 50Ω using inductive slots in the CPW ground which double as antennas for the second harmonic. Third, the fundamental will not radiate significantly, thereby providing a suppression of the fundamental that is not available from the previous design. Finally, angle tuning of the receiver may be used in addition to voltage tuning to find the optimum conversion efficiency. The proposed structure is shown in Fig. 5.8.

The work of this chapter has shown that the basic principle of phase-matching for second-harmonic-generation on a nonlinear transmission line, as demonstrated by Wedding and Jaĝer at low frequency is also applicable to generation of mm-wave radiation. The primary contribution of this work was a modification of the structure proposed earlier to allow phase-matched SHG over a broad electrical tuning range. It was also shown that microwave losses on the structure place an upper limit to the conversion efficiency that can be obtained. Spatial power combining should provide a significant improvement in conversion efficiency.

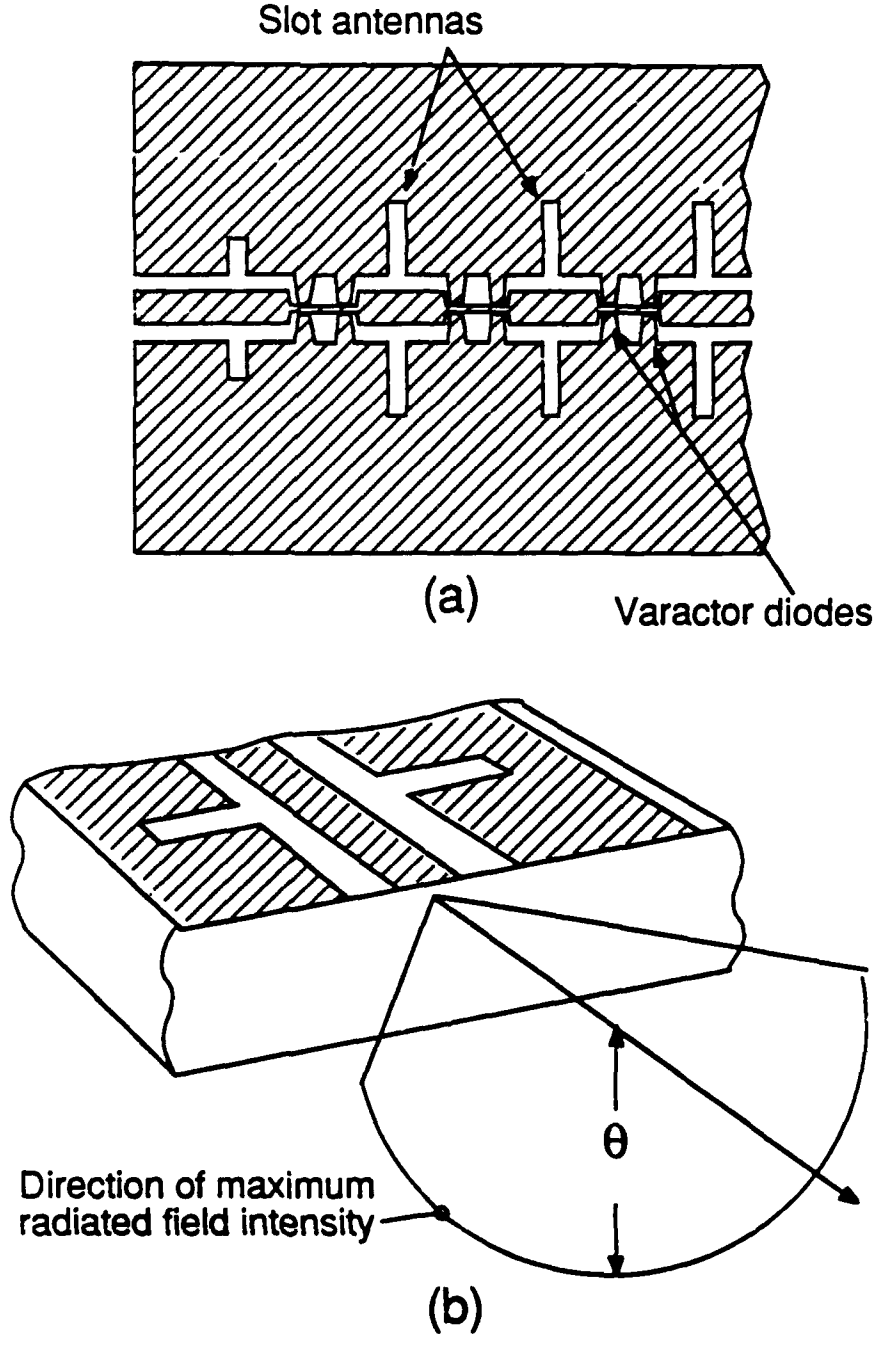

Figure 5.8: Proposed doubler using spatial power combining. The inductive slots in the CPW ground serve as inductors to the fundamental and antennas to the second harmonic (a). Radiation pattern is also shown (b).

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Chapter 6

Future directions

This thesis work has advanced the state of the art in sampler technology from 20 GHz to almost 300 GHz, while reducing the size and enhancing manufacturability. The sampler was then integrated with a resistive directional bridge to form the first S-parameter test-set on a chip. This chip exhibited approximately 10 dB of directivity to 60 GHz. Directivity can be improved with more precise resistor values. Finally, a monolithic distributed frequency multiplier was demonstrated with a 10 % conversion efficiency. With incremental improvements in performance, the directional sampler and distributed doubler technologies could reduce the price and enhance the performance of current mm-wave network analyzers. To exploit this technological advance over the bandwidths now available, it will be necessary to develop new approaches to probe fabrication and circuit interconnects, and to fully exploit the use of optical-IC hybrid systems.

6.1 Directional sampler rf probe

One of the advantages of the integrated circuits described here is that they are small enough to be mounted on probe tips. Bringing the measurement instrument into contact with circuit to be tested almost entirely circumvents the difficulty of interconnect losses. A proposed probe design for the directional sampler is shown in Fig. 6.1. With a ceramic probe tip, this approach should perform well to 100 GHz.

Ceramic probes with no active circuitry are commercially available with 65 GHz bandwidth [6.1]. A resistive multiplier assembled on a 5 mil Alumina probe tip has reached 130 GHz [6.2]. Above 100 GHz, the parasitics of the connection between the MMIC and the probe tip become intolerable and the tip must be eliminated. In this case, plated metal pads on the GaAs IC will be brought into direct contact with the circuit under test. Of course, the GaAs can not be allowed to flex, so the contact pressure must be applied by adding a specific weight to a balanced probe. .

This work is currently being pursued by Dan Van Der Weide and Mohammad Shakouri. The directional sampler discussed in chapter 4 and the associated IF circuitry are being placed on a microwave probe which will be useful to 65 GHz. Future modifications, coupled with improvements to the directional sampler design should allow operation to 300 GHz. Other circuits that will be probe mounted include the sampler for on-wafer time-domain reflectometry, the NLTL for a fast test signal generator, and the distributed doubler (also as a test signal generator). These on-wafer capabilities are most important for device designers because maximum frequencies of operation are already reaching 300 GHz [6.3]. Getting a detailed look at device operation above 60 GHz should provide new insight into device operation and limitations.

6.2 Circuit interconnects for operation to 300 GHz

The sampler and frequency multiplier designs presented here show that extension of broad-band measurement instruments to 300 GHz is feasible. However, one major barrier to the development of such instruments is the limited bandwidth of the interconnections. It is possible to design connectors and coaxial cables that operate single-mode to 100 and possibly 300 GHz by simply scaling down the existing components. However, such a scheme has two major problems. First, the small size required for single-mode operation makes the parts difficult to manufacture. For example, a coaxial connector that is single-mode to 300 GHz would have an

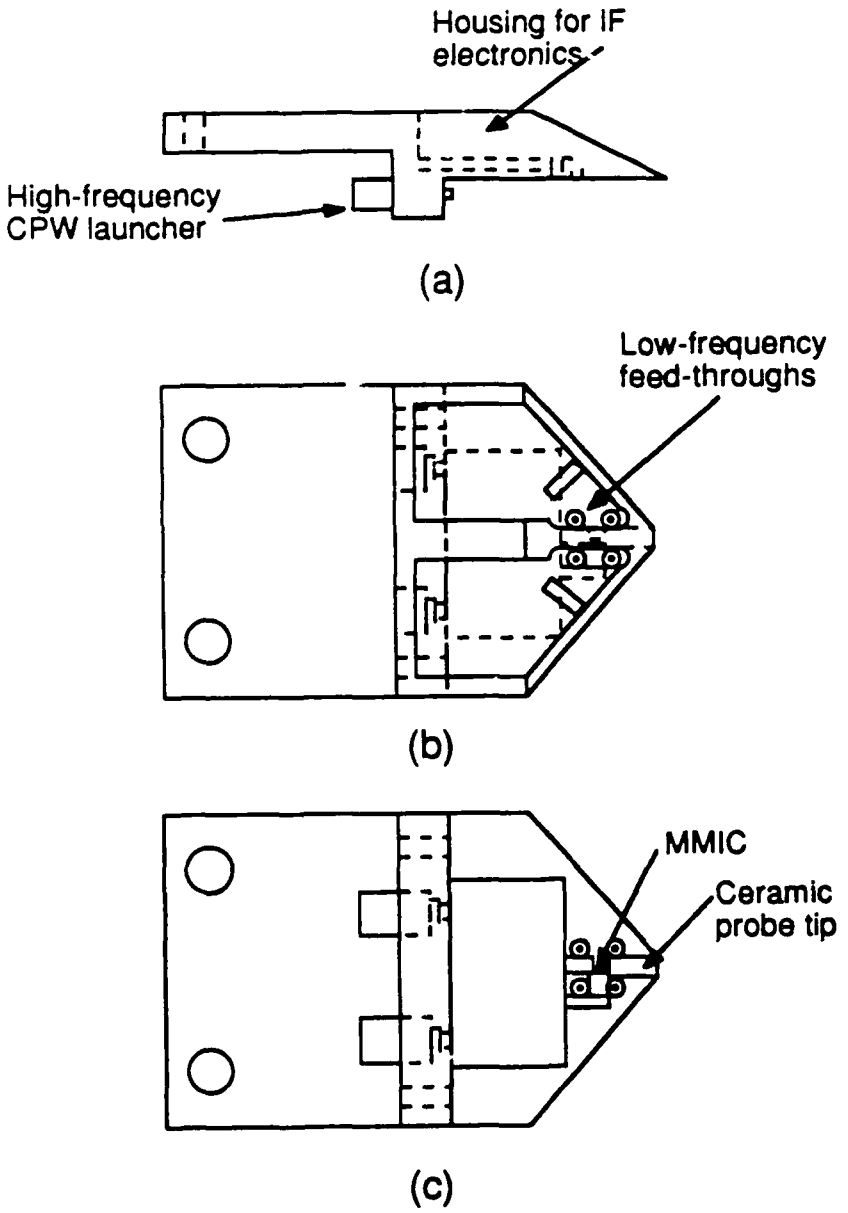

Figure 6.1: On-wafer probing with GaAs MMICs. A prototype active-probe directional sampler is shown in side view (a), top view (b), and bottom view (c). A ceramic probe tip can be used to 100 GHz, but may be abandoned to reach 300 GHz.

outer conductor diameter of 800 μm and an inner conductor diameter of 348 μm. Secondly, conductor losses increase with the square root of frequency and inversely with cable diameter, so a cable which is six times smaller and operating at six times the frequency will have 14.7 times more loss. This means a cable which has a loss of 1.5 dB/foot at 50 GHz and is single-mode to 60 GHz, will have a loss of 22 dB/foot at 300 GHz if scaled down to be single-mode to 360 GHz. In addition to conductor losses, dielectric losses tend to increase linearly with frequency at mm-wave frequencies because of the broad sub-millimeter absorption band in many dielectric materials [6.4]. It is interesting to note, however, that dielectric loss in GaAs is relatively constant to 250 GHz, before it begins to increase due to multi-phonon absorption near 600 GHz.

In the face of dramatically increasing conductor losses with increasing frequency in coaxial cable, engineers have traditionally turned to rectangular waveguide. For example, WR-3 guide has a theoretical attenuation ranging from 5.1 dB/ft to 3.5 dB/ft from 220 to 325 GHz [6.5]. However, it is extremely difficult to make a reproducible interface between a device such as a transistor or solid-state amplifier and the rectangular waveguide mode. The typical 40% waveguide bandwidth is often not large enough and waveguide dispersion makes it unsuitable for propagation of narrow pulses. Clearly there is a need for a low-loss, broad-band waveguiding structure that interfaces conveniently with solid-state devices.

One approach which is now widely used is to place a printed circuit transmission line inside of a hollow waveguide [6.6]. The printed circuit increases the bandwidth of the hollow guide and the hollow guide, by preventing radiation, allows larger conductors to be used on the printed circuit, thereby reducing the printed circuit conductor loss. An example of this type of line is the fin-line invented by Meier [6.7]. Fin-line is often used to provide a transition between the waveguide mode and a quasi-TEM planar transmission line such as microstrip which is used for microwave circuits. Fin-line, however, is not useful for connecting to circuits with many inputs and outputs.

Another approach is to accept high losses and simply reduce the length of the interconnect. This can be accomplished by combining the various components which

require broad-band connection on the same monolithic integrated circuit. This was the key to the success of the sampler presented in Chapter 3. Various integrated circuits can be connected together without lengthy interconnections by designing the ICs so that they may be brought into direct contact. This technique was employed for the Generation III sampler, with bond wires bridging the gap between the circuits. Alternatively, metal bumps could be plated on circuit input and output connections so the chips can simply be pressed together. However, higher levels of integration only postpone the eventual necessity of connection to the outside world. An interesting alternative to this final connection is the monolithic antenna. Patterning an antenna or array of antennas on the integrated circuit allows communication via free space propagation. Obviously, it may be difficult to use antennas for circuits with multiple inputs and outputs, but this approach has proven useful in several applications including high-power microwave generation [6.8] and radar transmit-receive modules [6.9].

Losses in existing waveguiding structures constructed of high-purity metals can be reduced by operating at a lower temperature. Resistivity due to phonon scattering decreases linearly with absolute temperature down to the Debye temperature Θ_D, where it begins to fall off even more rapidly, approaching $(T/\Theta_D)^5$ for $T \ll \Theta_D$ [6.10]. Thus, a metal film such as copper ($\Theta_D = 333K$) of sufficient purity at 85K would have a resistivity ten times lower than at room temperature. This means that if one is willing to suffer the expense of a liquid nitrogen cooling system and higher purity metals, drastically reduced losses can be achieved without significantly altering the circuit design or using a different metalization.

Finally, high-T_c superconductors offer the hope of even lower losses at mm-wave frequencies. According to the BCS theory [6.11], superconducting materials can have significant loss at mm-wave frequencies due to Cooper-pair breaking by the high-frequency fields. At frequencies above the frequency corresponding to the energy required for pair breaking

$$f_{gap} = \frac{3.54 k_B T_c}{2\pi\hbar} \tag{6.1}$$

where k_B is the Boltzmann constant and T_c is the temperature of the superconducting transition, the material reverts to normal conduction. Eq. (6.1) shows why

high-T_c superconductors are anticipated to be useful in mm-wave circuits. For example, a 90° T_c superconductor would have an f_{gap} = 6.65 THz. There is still considerable controversy over the applicability of BCS theory to the new high-T_c superconductors, nevertheless, theoreticians have already used the BCS theory to compare the possible performance of the new superconductors with conventional conductors such as copper [6.12]. If these predictions prove valid, a 90° T_c superconductor such as YBCO could offer lower loss than copper at 85K up to 500 GHz. The advantage of YBCO at 100 GHz would be perhaps a factor of ten. However, recent experimental measurements of surface resistance on 2000Åthick YBCO have shown no advantage of this material over gold for frequencies above 100 GHz [6.13]. It remains to be seen whether thicker, higher quality YBCO films will achieve the advantage predicted by the BCS theory.

6.3 Optical synthesis

Another method of circumventing lossy interconnections is to place the mm-wave signal on an optical carrier. A photodiode receiver could then be integrated with the circuitry on-chip. The bandwidth available on an optical carrier is tremendous. This perspective brings a new challenge to measurement technology: how to achieve bandwidths that are significant in comparison to the optical frequency of todays communication systems, 194 THz. The possibility of such broadband detection is illustrated by the metal-insulator-metal (MIM) diode. This device has been used for signal rectification up to 197 THz for optical frequency synthesis and measurement [6.14]. If this detector was combined with a sampling receiver, a frequency synthesizer could be constructed that is tunable over a sizable optical bandwidth.

The nonlinearity of the MIM diode is due to the quantum-mechanical tunneling of electrons through the barrier created by the thin insulator. In the common W-Ni diode, the insulator is nickel's native oxide. The device is usually assembled much like a crystal radio detector where the tungsten is a 2 μm whisker that is electrochemically etched to form a 1000$\AA$ tip which is then brought into contact with the nickel sample using a micro-positioner. Attempts have been made to pattern

them monolithically [6.15]. However, the technology now exists for micro-machining tungsten tips on silicon wafers. These tips can have 500 to 100$\AA$ radii of curvature [6.16]. The smaller tip area may permit the MIM diode to be used well above 197 THz, while the micro-machined structure may permit the integration of an array of MIM diodes with a sampling receiver. Thus the frequency difference between two optical sources could be detected without the use of a small band-gap material for electron-hole pair production. An example of such a system is shown in Fig. 6.2. The synthesized output can be used as a local oscillator for a high resolution spectrum analyzer, or the combined synthesized and reference outputs can be used as a source of mm-wave radiation.

The MIM diode provides the possibility of huge bandwidths. However, the conventional photodiode has also made significant progress in recent years. In the popular 1.3 and 1.55 μm communications bands, the preferred detector material is InGaAs on InP. Detectors in this material system have reached 67 GHz [6.17]. For visible radiation, the more mature GaAs technology detectors have reached 100 GHz [6.18] with a quantum efficiency of 25%. Since quantum efficiency can be traded directly for bandwidth in a conventional vertical photodiode [6.19], the bandwidth can be increased significantly in applications where sensitivity is not of primary importance.

When the signal is delivered to the chip on an optical carrier, the bandwidth is only limited by the on-chip circuitry. For example, suppose a sampler is integrated with one or more diode detectors (MIM or photodiode). Utilizing the techniques developed here, a sampler having a 1 THz GHz 3-dB bandwidth should be feasible. If the transmission lines connecting the detectors and the sampler are less than 100 μm long, the detector – sampling receiver combination could also approach a 3-dB bandwidth of 1 THz. Using this sampling receiver in an optical synthesizer would provide an 80$\AA$tuning range at 1.55 μm wavelength.

Another application for this sampling photoreceiver is electrooptic sampling. This technique, discussed in Chapter 1, uses an ultra-fast pulsed laser to achieve picosecond time resolution. However, the techniques used to produce the ultrafast pulses, such as mode-locking and pulse compression, also contribute to intensity

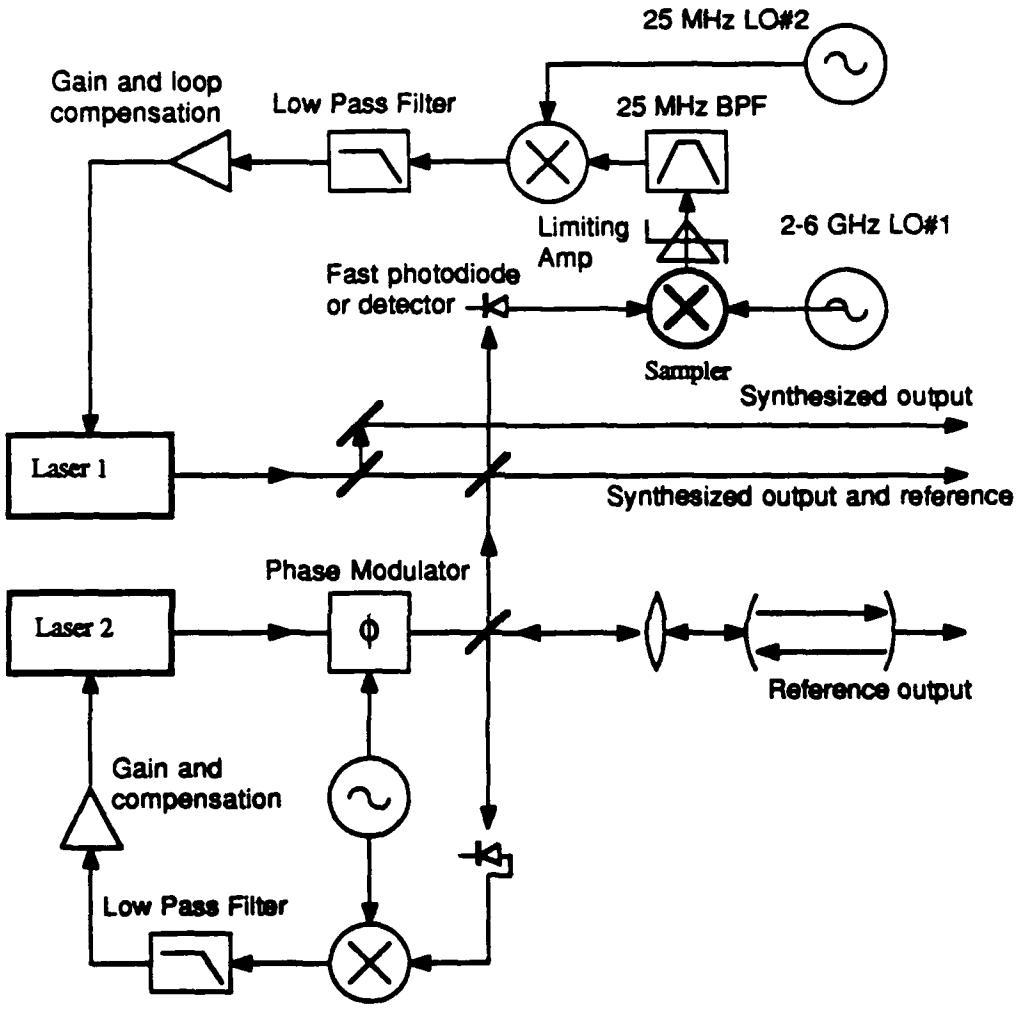

Figure 6.2: Optical frequency synthesizer block diagram.

noise on the laser beam. In addition, it is very difficult to stabilize the pulse repetition rate to the degree necessary for low phase-noise measurements at mm-wave frequencies. If the pulsed laser were replaced by a continuous-wave laser that was amplitude and frequency stabilized, the received electrooptic signal would be nearly shot-noise limited. The 1 THz photoreceiver and its microwave local oscillator would then set the time resolution of the system. It is interesting that the high-speed sampler technology that was motivated in part by the picosecond time resolution made possible by the ultra-fast laser could render it obsolete.

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